Technical Update

May 2011

DCG Systems

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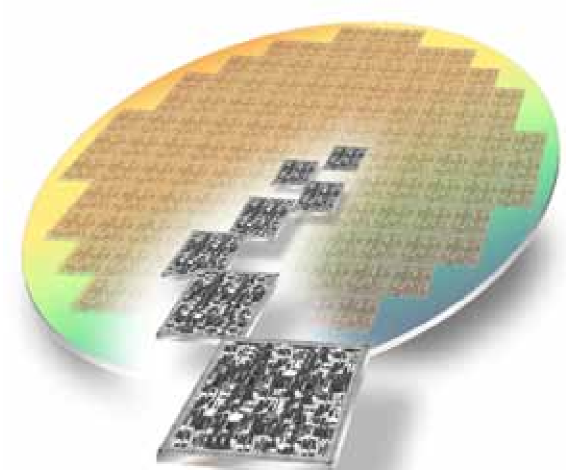
Upcoming Events

- 16-17 June - DCG KK's Technical Forum, Shin Yokohama, Japan
- 4-7 July 2011 - DCG booth at the18th International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), Songdo Convensia, Incheon, Korea
- 3-7 Oct. 2011 - 22nd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF), Bordeaux, France
- Oct. 2011 - DCG's ESREF Technical Seminar
- September 2011 - DCG's Korea Technical Seminar
- 20-22 September 2011 - DCG booth at International Test Conference (ITC), Anaheim, California
- 9-11 Nov. 2011 - LSI Testing Symposium (LSIT), Japan
- 13-17 Nov. 2011 - 37th International Symposium for Testing and Failure Analysis (ISTFA), San Jose, California
- 18 Nov. 2011 - DCG's After ISTFA Technical Seminar

The Rise of Wafer-Level Electrical Failure Analysis

Dealing with Moore's Law

Moore's Law states that the number of transistors that can be fit on an integrated circuit will double every two years. Manufacturers are beginning to produce and debug 22nm technologies. Devices are operating faster at lower power, with supply voltages moving well below the 1-volt level. Sub-volt signals become lost in device noise, making the extraction of signal information even more challenging.



Failure Analysis is rapidly moving from the realm of single-die to the wafer.

Wafer yields are decreasing due to a new array of problems that were not apparent at previous technology nodes. The physics of device operation introduce new types of "soft" defects which cannot be seen unless the device is operated at speed under the right conditions. The days in which we could quickly and reliably locate a fault using simple emission or straightforward probing are behind us.

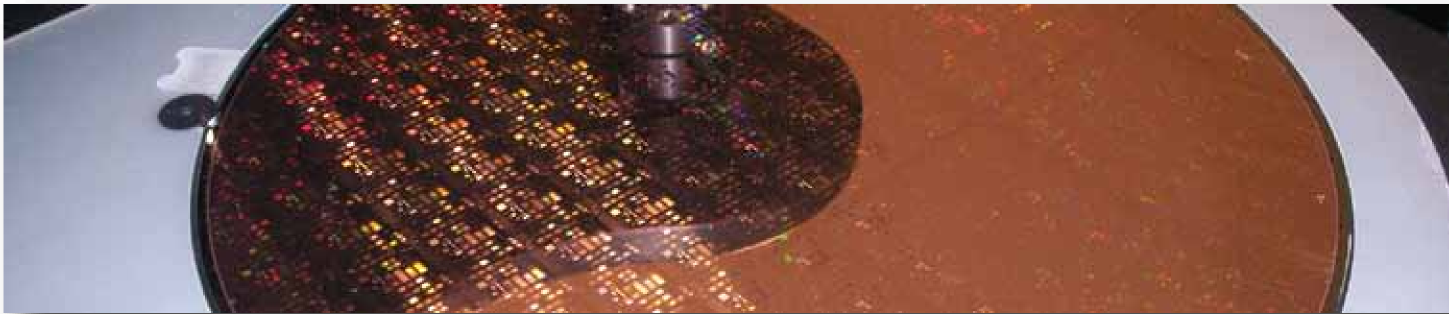
With a higher number of chips on a single wafer, the need to maintain high wafer yields becomes even more critical in order to be able to maintain a competitive edge and achieve time-to-market. Wafer analysis has become a process of determining design marginality rather than a search for a physical artifact.

The *International Technology Roadmap for Semiconductors* (ITRS) 2009 notes the following trends related to wafer yield:

- "As the number of steps, the number of transistors, and the circuit density increases, and the critical defect size decreases, an increasing number of defects are only seen as electrical faults." (ITRS 2009, p. 7)
- "Increasing yield loss due to non-visual defects and process variations requires new approaches in methodologies, diagnostics and control. This includes the correlation of systematic yield loss and layout attributes." (ITRS 2009, p. 4)
- "As circuit design becomes more complex, more circuit failures will be caused by defects that leave no detectable physical remnant" (ITRS 2009, p. 6)
- "It is a challenge to find small but relevant defects under the vast amount of nuisance and false defects" (ITRS 2009, p. 4)

Design versus fabrication

The boundaries between circuit design and circuit analysis have become blurred. There is more to performing an efficient wafer analysis than simply having the ability to acquire huge amounts of emission data. The data on each die of the wafer must be correlated in a manner that allows the analyst to distinguish between random defects and systematic defects. Invisible faults may be process related, or they may be design related. In all



Wafer-level analysis is the first line of defense in order to determine the cause of "invisible" defects.

likelihood, however, they are some combination of both. Designers and device analysts can no longer occupy separate domains - they must work together in order to conquer the new yield challenges. The need now exists for an effective method of performing dynamic Electrical Failure Analysis (EFA) at the wafer level.

Protecting intellectual property

The increased dependency on design information for high resolution fault diagnostics poses a particular challenge for yield collaboration between design houses and foundries.

Design houses wish to release as little information as possible to the foundry regarding the circuit schematic, and will not send anything related to the device schematic to the foundry. Typically, they are limited to sending only physical X-Y coordinates to the foundry. Unfortunately, this limited information is not sufficient for locating speed-dependent "invisible" defects.

Likewise, the foundry will not release data to the design house regarding process-related issues. The mutual desire on the part of design houses and foundries to protect both design and process details creates an information bottleneck that can seriously hinder the analysis process for leading-edge technologies.

Fault diagnostic software

Predictive software methods which utilize the electrical netlist allow the design house to narrow down the search for a fault. The production tester runs functional test and structural tests on a failing device, which generates a data log or a test log. This data log is then fed into a "fault diagnostic" program which uses the device netlist to generate a set of possible failure locations within the circuit logic. This may be run entirely on the design side, thus protecting design IP from being released to the foundry. The result, however, is ultimately an educated guess as to the true location and nature of the fault. The fault diagnostic is a vital step in the process, but finding the exact cause of failure requires further analysis using the original design data. This can require passing a design-derived range of suspected fault locations back to the foundry.

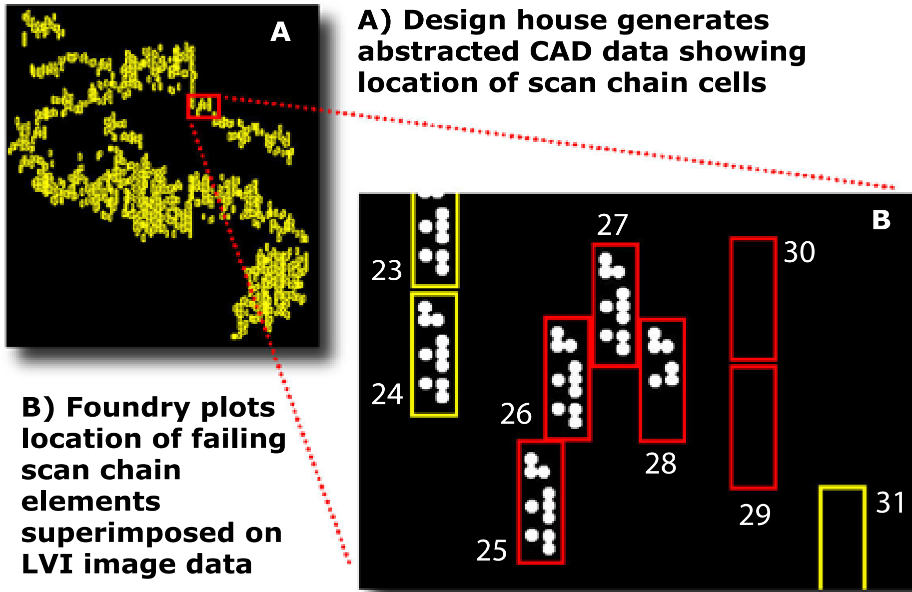
Design house/foundry data exchange is crucial to the success of the analysis.

Design data abstraction

A solution to the problem of providing the foundry with sufficient design information for physical analytical purposes is achieved by abstracting the relevant design data. The use of abstracted design data protects IP, while allowing the foundry to utilize a mapping of logical elements to physical coordinates in order to identify process-related issues without having to release details of the process to an outside entity. This is done by making use of design files that have been stripped of proprietary information such as cell and net names. These files provide spatial information about the design which is invaluable to the analyst, yet prevent the design itself from being reverse engineered. The foundry is thus able to analyze complex failures using advanced emission and laser-based techniques such as Laser Voltage Imaging (LVI).

Using scan-chains to identify process defects at wafer test

Consider the case of scan-chain failures that occur at wafer test. These failures are typically ignored as unsolvable at this stage of production. Wafers showing scan-chain failures are simply discarded, thus lowering overall yield, and more importantly, yield learning. Significant analysis of potential process-related defects may not occur until the wafer has been diced, and the individual devices packaged. By utilizing abstracted CAD data coupled with LVI, these failing wafers now become a critical first line of defense in the battle for yield. The ease with which the LVI analysis can pinpoint the precise location for the Physical Failure Analysis (PFA) makes the diagnosis of such failures at the wafer test stage entirely feasible. Diagnosing early scan-chain failures identifies process related issues significantly early in the fabrication process.



A) Design house generates abstracted CAD data showing location of scan chain cells

B) Foundry plots location of failing scan chain elements superimposed on LVI image data

Design house runs fault diagnostics to identify failing section of scan chain. Abstracted scan chain CAD data is sent to the foundry. Foundry analyzes scan chain using CAD data and LVI to locate failing element. White circles represent LVI data from individual transistors in the scan chain flip-flop. Scan element #28, which visually shows partial LVI activity, is the location at which physical analysis must be performed.

Design data abstraction is particularly useful for assisting the design house and foundry in performing wafer-based scan chain analysis using LVI. After chip tape-out, the design house generates all scan chain physical maps, replaces each proprietary hierarchical instance name with an ordered number, and then provides them to the foundry for later use during analysis. When a particular die on the wafer fails the scan chain integrity tests, the foundry sends the test data log back to the design house for identification of the failing chain. If the design house runs ATPG software on the design, they can provide a range of suspected failing scan-chain elements back to the foundry.

The foundry loads the physical layout into the CAD navigation tool. A Laser Voltage Imaging (LVI) tool capable of visually imaging scan chain activity is aligned with the CAD display. The analyst focuses attention on the range of suspected failing scan chain elements and visually locates the failing element. Physical analysis is then performed at the correct location.

Physical failure analysis guided by wafer-based scan-chain debug using LVI has turned what was once a significant low-yield liability into a early warning analysis technique that has proven to be over 90% effective.

Focus on the Field: Elaine Cheng

Elaine Cheng received her Bachelor's Degree in Physics from National Chung Hsing University (NCHU) and her MS-EE from National Taiwan University (NTU). She worked for Integrated Service Technology (IST) for 8 years as an Engineer for FIB and SEM Applications.

Elaine worked for Spirox for 7 years as a Circuit Edit Applications Engineer to support DCG product lines. Since July 2010 Elaine has been a Applications Support Engineer (Field application & customer support engineer) for DCG Taiwan covering circuit edit, nano-probing, EFA, EDA and yield learning.

With 6 years experience working with the OptiFIB II/III/IV on the circuit edit operation and application, Elaine successfully assisted the very 1st WaferScan demo project in Taiwan and earned her customers' respect while she was still with Spirox.

Elaine loves outdoors activities such as swimming, surfing and snorkeling. She likes to watch baseball, basketball, and spend time with her two lovely Beagles. Elaine loves travel to other countries to explore different parts of the world whenever she gets the chance.

Technical Information from DCG Seminars

DCG's 2011 Taiwan Technical Seminars

In February, DCG held two very successful technical seminars. Our first seminar, held at TSMC had 35 people attending. Our public seminar the following day at National Chiao-Tung University had more than 150 attendees. Presentations at these seminars included:

- "Volume Electrical Failure Analysis for Product-Specific Yield Enhancement " (NVIDIA)
- "Data Exchange between Design House and Foundry in Yield Analysis" (DCG)
- "Sensitivity and Resolution in Photon Emission Microscopy" (DCG)
- "Through Package Defect Localization by Lock-In Thermography" (DCG KK)
- "Isolation of Fault found at Wafer Electrical Test using PEM, EBIC and Nano-probing" (DCG)
- "Addressing Circuit Edit Challenges at 22nm and Beyond" (DCG)

These presentations may be downloaded from the DCG website.

ELITE data presented at conferences

Rudolf Schlangen presented a paper titled "Through Package Defect Localization by Lock-In Thermography," at the 7th International Conference and Exhibition on Device Packaging, Scottsdale/Fountain Hills, Arizona USA. This paper focused on the use of Lock-in Thermography as an effective means of diagnosing defects within stacked-die packages.

Antoine Reverdy of Sector Technologies presented ELITE data at the System, Software, SoC and Silicon Debug (S4D) workshop held in Grenoble, France on 14 March 2011.

Semicon China

In March, DCG participated at Semicon China with its partner Spirox.

ISTFA 2010 Best Paper

Best Paper: *Electron Beam Absorbed Current as a Means of Locating Metal Defectivity on 45nm SOI Technology* by Dickson, Erington, Lange, and Ybarra of Freescale.

Call for papers for LSITS 2011

Papers are being requested for presentation at the LSI Testing Symposium, Osaka, Japan, 9-11 November 2011. Abstracts must be submitted by late August. Papers may be submitted in either Japanese or English. Those interested in submitting a paper should contact LSITS@ist.osaka-u.ac.jp

The 2011 annual Lantern Festival celebrates the "Year of the Rabbit." DCG Taiwan Technical Seminar at National Chiao-Tung University had over 150 attendees.

DCG Systems
DCG Systems, Inc.
45900 Northport Loop East
Fremont, CA 94538
Tel: +1 510 897-6800 | Fax: +1 510 897-6801
www.dcgsystems.com