Technical Update

November 2010

DCG Systems

In this issue...

News and Events

Upcoming and recently presented conference papers

- "Enhanced Lock-In Thermal Emission," (DCG K.K., DCG Systems) LSI Testing Symposium 2010.
- "Laser voltage imaging for ATPG scan chain diagnosis on 40 nm CMOS," (NVIDIA, DCG Systems, DCG Systems K.K.) LSI Testing Symposium 2010.
- "Made use of N-well layers for advanced backside circuit edit," (DCG Systems K.K.) LSI Testing Symposium 2010.
- “Application of Lock-in Thermography on PCB for Fault Localization and Validation of Failure Mechanism Due to External Discrete Component Variation,” (National Semiconductor, DCG), ISTFA 2010.
- “Novel Pulsed Spot Milling Technique to Extend Gallium Ion Beam Technology for Circuit Edit,” (Intel, DCG) ISTFA 2010.
- “Novel Circuit Edit Solution for Bulk Cu Milling,” (Maser, DCG) ISTFA 2010.
- “Two-Photon X-Variation Mapping Based on a Diode-Pumped Femtosecond Laser,” (Heriot-Watt University, DCG) ISTFA 2010.
- “Laser Voltage Imaging: A new Perspective of Laser Voltage Probing,” (NVIDIA, DCG) ISTFA 2010.
- “Developing a Chemistry-Assisted Focused Ion Beam Process for ‘On-Demand’ Solid Immersion Lenses in Silicon (Berlin University of Technology, DCG) ISTFA 2010.
- “Volume Electrical Failure Analysis for Product-Specific Yield Ramp,” (NVIDIA, DCG) ISTFA 2010.
- “Fault Isolation of Sub-Surface Leakage Defects Using Electron Beam Induced Current Characterization in Next-Generation Flash Memory Technology Development,” (Spansion, DCG) ISTFA 2010.

Efficient use of design data for logical/physical cross mapping

CAD navigation has been an integral part of device analysis since the early days of E-beam probing. The idea that CAD design files could be linked to a physical X-Y stage in order to move a device to a desired location or locate an emission spot was a revolutionary breakthrough. Gone were the days of needing to laboriously generate paper plots of the GDS2 physical layout, hanging them on lab walls and painstakingly tracing one’s way through a labyrinth of metal layers in order to determine where to even begin probing. In 1988, the IDS 5000 E-beam prober’s 500MB disk option occupied a pedestal that was 2-feet high, 2-feet deep and 1-foot wide. Nobody even imagined how such a vast amount of space could ever be filled with CAD data!

Looking back to that time from now, when we now routinely carry 16GB flash drives on our keychain, or have 2TB external backup drives for our desktops, it is easy to see just how far things have progressed over the past 22 years in terms of data storage ability. As can be expected, however, increasing disk space and more powerful microprocessors came with a corresponding increase in CAD design size and complexity.

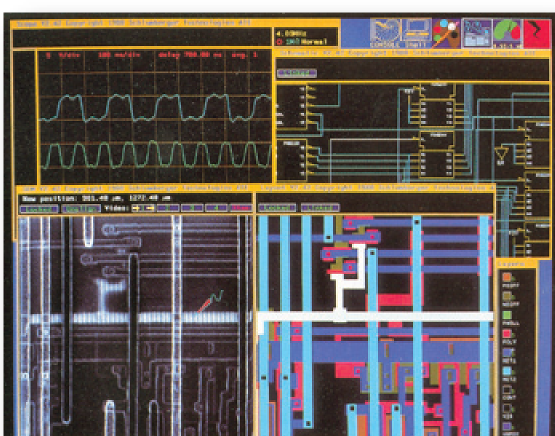


Figure 1: The way things used to be in 1988: CAD navigation on the original IDS 5000 linked the GDS2 physical layout design to the SEM image

In 1988, it was possible to perform a complete cross-reference of the physical layout in the GDS2 file with the netlist (Layout versus Schematic or “LVS”) comparison in just a few hours, in order to create a complete cross mapping of schematic elements to their physical counterparts that could be used by the device analyst.

Evolving beyond LVS

Usability of LVS results for the purpose of device navigation began to break down with the advent of multi-gigabyte designs. Although computer speed and memory have increased significantly, the increase in design complexity has far outpaced them. It was no longer feasible to simply "scale upward" and use the same, node-by-node approach to create a cross-reference map. LVS became impractical for all but a handful of companies that had the infrastructure in place to support these large conversions. While it was perfectly acceptable to spend a few hours processing a LVS design in 1988, it became unacceptable to spend an entire week processing a design in the same manner in 2005. In addition, these conversions usually require an in-house expert. The needs of the device analyst to have the navigation data ready as soon as possible did not change, but the amount of time required to produce that data did. It was possible to actually obtain emission data more quickly than it was possible to create the CAD data needed to locate a particular photon or thermal emission spot. An alternative method of quickly producing navigation data for the device analyst was urgently needed.

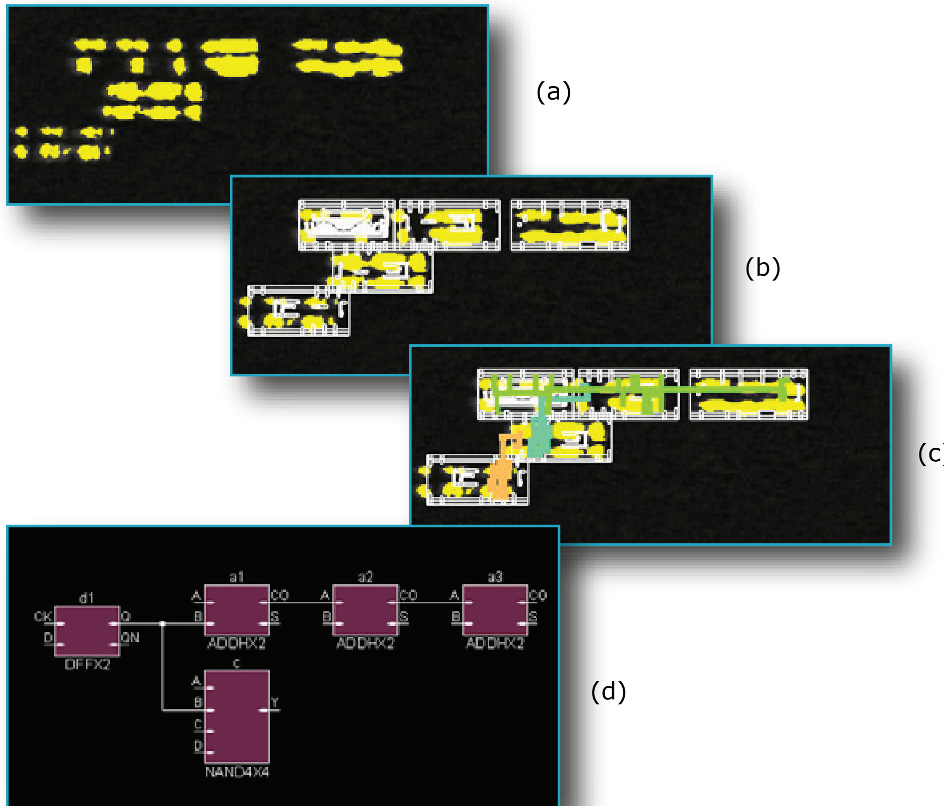


Figure 2: (a) Colorized LVI image, (b) SiGPS cell data superimposed on LVI image, (c) Net trace data obtained directly from the physical GDS2 layout showing connections between highlighted cells, and (d) Logic cone corresponding to the physical logic block shown in (a), (b) and (c).

Using place-and-route data for cross mapping

In 2005, a new method for processing CAD navigation data was introduced. This involved the use of existing place-and-route data for standard cell designs. These design files, based upon Cadence's Library Exchange Format (LEF) and Design Exchange Format (DEF), already contained all of the information required in order to create an effective cross mapping file for device navigation in logic blocks. The LEF file contains information related to cell library used in the design, most importantly the location of the pins in each cell. The DEF file contains the cell placements and orientations, in addition to the routing between the cells. Together, these files, when superimposed on the GDS2 physical layout, provide a quick and easy method of producing navigational data for the analyst in order to locate emission spots. What was needed was an algorithm which could create a searchable database linking together all of the LEF and DEF information for a design. The engine developed for this purpose was called Silicon GPS (SiGPS). Now, rather than spend days attempting to perform LVS on a design, it became possible to produce cross-mapping in a very short amount of time. More importantly, the DEF annotation (i.e. hierarchical instance names) more closely matched the names used in DFT and front-end design tools.

Although processing LEF/DEF place and route information appeared to solve a great number of problems that were not addressed by LVS, the processing of the DEF files was dependent upon the size of the design. A larger, more complex design required correspondingly larger DEF files. For example, a 50GB DEF database would require less than a day to process *only* the cells, but would require an entire week to process cells *and* nets. A faster way of obtaining net connectivity between cells, preferably "on-the-fly," was needed.

Hybrid approach

The solution to the problem of increasing LEF/DEF processing times lies in the use of a combination of elements from both the GDS2 physical layout and the LEF/DEF approach. By using the DEF cell placement and LEF port data, and combining with an electrical net trace in the GDS2 physical layout, it becomes possible to achieve navigation times which are truly efficient. Ignoring the time consuming DEF routing allows us to avoid an overly significant amount of pre-processing of the navigation data. In essence, it becomes possible to take advantage of the "best of both worlds" using the LEF/DEF data as well the physical design net tracing from the GDS2 file.

Net tracing uses only the physical design information contained in the GDS2 file, including layer information and electrical interconnection, to fully highlight the logical components coinciding with an emission spot. This is a feature that is available when LVS is performed, but in the case of net tracing, the determination of the electrical connectivity is performed "on-the-fly" at the time that the net trace query is made when used to determine the location of photon emission or voltage modulation from Laser Voltage Imaging (LVI) analysis. (See DCG Technical Update November 2009)

When net tracing is combined with LEF/DEF component queries, an effective "physical design aware" logic cone tracing is achieved. This is particularly effective when used to trace the fan-in or fan-out of a cell with an emission spot or abnormal LVI activity. The analyst overlays CAD with the emission or LVI image, then highlights the logical components at the emission using the SiGPS LEF/DEF query engine. The logical cell and pin data are superimposed on the emission or LVI image. Selecting a pin automatically highlights the connected physical net using only the GDS2 layout, and annotates this net with the LEF/DEF cell/pin name. The highlighting of the physical net does not utilize any pre-processed place-and-route data (LVS or other method), but instead uses the available GDS2 physical design information. Once the net is highlighted, it is possible to quickly identify all of the connected cells.

Devices will, without a doubt, continue to become more complex, with timely production of cross mapping data an essential part of the analysis process. DCG will continue to explore even more efficient methods to keep pace with technology trends.

MASER Engineering wins award for work with OptiFIB-IV

MASER Engineering has won the 2010 Euroasia Industry Awards in the category of Fab Management support. The award was presented based upon the work done by MASER's sub-100 nm circuit edit services performed using their DCG Systems OptiFIB IV system. The award was presented during Semicon Europe 2010.

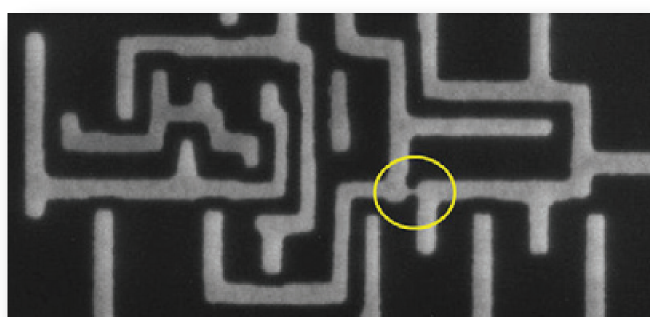
EuroAsia Semiconductor Magazine notes: "The new OptiFIB-IV system has led to MASER receiving the FAB Management Award in the IC Industry Awards. The system has unique features designed to support fabless IC manufacturers." [1] The article goes on to list unique features of the OptiFIB-IV, such as the coaxial optical/ion column, dual chemistry injection nozzles and advanced end-point detection. The OptiFIB-IV also offers the "best copper edit chemistry solution in the industry."

[1] "Circuit Edit service for sub-100nm IC technology designs," EuroAsia Semiconductor Magazine, Issue IV, 2010, p. 14. www.euroasiasemiconductor.com

Kees Revenberg of MASER Engineering receives the 2010 EuroAsia Industry Award for Fab Management support from Stephen Whitehurst, COO of Angel Business Communications Ltd.

A lock-in thermography success story

One of our customers recently reported his success using the DCG ELITE lock-in thermography system. The customer was experiencing a high Icc standby problem on one of their devices. The first attempt at resolving the issue involved using their own Hypervision emission detection system. Unfortunately, the system (with thermal camera) was unable to detect any thermal "hotspot" which could have pinpointed the location of the fault. The customer suspected that this could be a backend problem which could be diagnosed at the wafer level. The customer then solicited DCG's help to examine the wafer using the ELITE lock-in thermography system. Within just a few days the customer had their wafer on the ELITE demo system at DCG Fremont. The customer brought in their own probe card and benchtop tester and quickly brought up the device on the ELITE. Within a short time, they were able to observe a consistent hot spot on many different wafer die within just half a day. According to the customer, they "nailed the root cause the very next day." The defect turned out to be a bridging fault between two metal lines. Ultimately, the ELITE was used to quickly solve a problem that could not be located using a standard emission tool, even with thermal sensitivity.



Customer device showing the bridging fault between two metal lines that was discovered using the ELITE lock-in thermography system.

ESREF 2010 and DCG Technical Seminar

DCG and SECTOR Technologies jointly participated in the 21st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) held in Gaeta, Italy. DCG and SECTOR also held a technical seminar. The following seminar presentations were offered:

- **Enhanced Thermography**: Fault localization and thermal analysis solution using ELITE.
- **Laser Voltage Imaging:** Specific use for security and reverse engineering investigations.
- **Sierra**: New software platform across DCG EFA tools - demo on DCG Systems Meridian.
- **SEM Nanoprobing**: Example of sProber applications and transistor characterization.

SECTOR and DCG personnel at the ESREF booth

Focus on the Field: Brian Pollock

Brian Pollock began his working career as a manufacturing engineer at a company that manufactured time clocks. From there, he got a job working as a field engineer with a company that made welding robots and high speed circuit board assembly equipment. In his 5 years there he traveled the world visiting all sorts of manufacturing facilities and locations.

After a brief stint as a field engineer installing and maintaining vertical diffusion (CVD) and atmospheric vertical diffusion (AVD) furnaces, Brian joined Schlumberger's Automated Systems Group in 1995 as a on-site resident field engineer for Schlumberger's device handlers, performing scheduled PMs and remedial repairs to an installed base of over 150 device handlers, burn-in loaders and inspection machines.

In early 2000, Brian transferred to Schlumberger's test group as the field service manager for the southwest region. This job expanded to include the Costa Rican Field Service Group as well as oversight of local resources and collaboration with the accounting and legal teams to maintain the company's presence in Costa Rica

The Schlumberger ATE division eventually became NPTest, which later became a division of Credence. As operations wound down in the test group, Brian accepted his current position as Eastern Region Field Service Manager with DCG. Brian currently manages the Eastern Region for DCG with 9 field service engineers reporting to him.

Brian is married with 3 teenage kids. With two of those kids in high school marching band, this time of year his weekends are full of helping out the marching band wherever possible.

One of Brian's other duties is to manage DCG's Customer Relationship Management (CRM) software. This is the place where DCG Field Service Engineers go to record activities on systems, order parts and track special projects. With a fully adaptable CRM, Brian has been able to create methods of tracking machine downtime, part quality and other field events. Having the data available to track our service business has allowed DCG to improve in all areas of service.

As Brian approaches 15 years of service, his knowledge continues to improve and grow. While mainly focusing on day to day management of field operations, he helps out wherever and whenever necessary, taking on special projects and doing whatever it takes to get the job done.

About six years ago, Brian saw an ad in a local newspaper for a community orchestra that was starting up. Brian was an avid tuba player in high school and realized that performing music was something he truly missed doing, so he bought a tuba and has been performing with the group ever since.

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