

## Jitter analysis of PLL-generated clock propagation using Jitter Mitigation techniques with laser voltage probing

Joy Y. Liao<sup>a,\*</sup>, Tung Ton<sup>a</sup>, Nathan Slattengren<sup>a</sup>, Steven Kasapi<sup>a</sup>, William K. Lo<sup>a</sup>, Howard L. Marks<sup>a</sup>, Yin S. Ng<sup>b</sup>, Ted Lundquist<sup>b</sup>

<sup>a</sup> NVIDIA Corporation, 2701 San Tomas Expressway, Santa Clara, CA 95050, USA

<sup>b</sup> DCG Systems Inc., 45900 Northport Loop East, Fremont, CA 94538, USA

### ARTICLE INFO

#### Article history:

Received 30 June 2009

Available online 29 July 2009

### ABSTRACT

A new Jitter Mitigation feature in the latest generation laser voltage probing (LVP) tool effectively removes PLL jitter from LVP waveforms [Ng Yin S, Lo W, Wilsher K. Next generation laser voltage probing. In: Proceeding, international symposium on testing and failure analysis; 2008. p. 249]. It facilitates the probing of phase-locked loop (PLL) driven circuitry inside of integrated circuits (ICs). In particular, it allows the detection of small amounts of excess jitter that would normally be masked by the much larger jitter of the PLL. To demonstrate the practical application of this Jitter Mitigation feature, we report on the jitter analysis of a PLL-generated clock signal as it propagates, through buffers and logic circuitry, to an external I/O pad of an IC. The IC was a 0.9 V, 65 nm technology graphics processing unit (GPU). The analysis was to determine where excess jitter was introduced into the clock path when the GPU was electrically stressed. Details of the jitter analysis, including Jitter Mitigation methodology, probing setup, and results of the timing measurements, will be presented in this paper.

© 2009 Elsevier Ltd. All rights reserved.

### 1. Introduction

Excess jitter was found on one of the clock outputs of a GPU when it was electrically stressed. Electrical characterization of the GPU revealed that the other clock outputs generated by the same PLL did not exhibit excess jitter. This indicated that the excess jitter was not generated in the PLL itself, but was injected somewhere along the clock signal path. Period jitter measurements made electrically at the external I/O pin showed that jitter increased from 37 ps (full width at half maximum, FWHM) in idle mode, to 54 ps when the chip was fully stressed. Assuming random jitter sources, the excess jitter is calculated to be:

$$\sqrt{(54 \text{ ps})^2 - (37 \text{ ps})^2} = 39 \text{ ps (FWHM)}.$$

An LVP analysis was undertaken to identify the location along the internal clock path where this extra 39 ps of jitter was introduced. The latest generation LVP tool was selected because of its new Jitter Mitigation feature, its high intrinsic bandwidth (up to 20 GHz) and its low-voltage probing capabilities ( $V_{dd} < 0.5 \text{ V}$ ).

In traditional LVP, the signal of interest is acquired in reference to a separate electrical trigger signal that is provided to the probing tool [2]. This trigger is usually generated by an automated test equipment (ATE) tester, or is derived from the crystal oscillator of a system applications board (hereafter, both will be referred to

as the device under test stimulus). The stimulus also provides the reference clock signal to the device under test (DUT). The trigger signal is therefore synchronous with, and coherent to, the DUT's reference clock.

On-chip PLLs are typically used to derive higher frequency core-clock signals from the provided reference clock. Since PLLs invariably introduces jitter between its reference and output clock signals, waveforms acquired using a traditional LVP tool on circuits driven by a PLL will have the PLL's jitter embedded in the acquisition. Because PLL jitter is usually the dominant form of jitter in a chip, it can mask the jitter from other sources.

Jitter Mitigation provides a solution to this problem by enabling the LVP system to be triggered by an edge of another clock reference. This new clock effectively becomes the timing reference and all jitter measurements are made relative to that clock. For example, if a direct output from the PLL is available, the PLL clock can become the timing reference for LVP measurements.

In this paper we took a slightly different approach. As a direct output of the PLL was not available, the output of the clock tree that was exhibiting the excess jitter was used as the timing reference, requiring us to work backwards towards the jitter source. Details are presented in the following sections.

### 2. Period jitter

Period jitter (Fig. 1) is defined as the maximum change in a clock's output transition from its average, and is typically quoted

\* Corresponding author. Tel.: +1 408 486 7306.

E-mail address: [jliao@nvidia.com](mailto:jliao@nvidia.com) (J.Y. Liao).

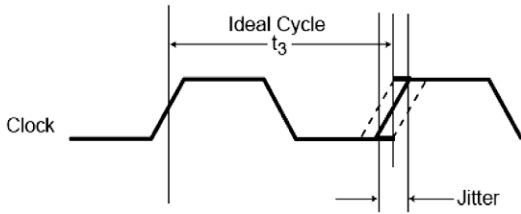


Fig. 1. Definition of period jitter: the deviation of the period from the average period.

as a peak-to-peak value for deterministic jitter to indicate the maximum change in the clock period. Root mean square (RMS) values are typically used if the jitter source is random. Random jitter follows a normal distribution and is not bounded by a simple peak-to-peak value.

Period jitter is measured electrically using an oscilloscope by triggering on one clock edge and setting the time-base parameters to display the next corresponding edge. Traces are accumulated using a long persistence value of the oscilloscope and a histogram is generated of the crossing point of the edge. Jitter parameters, including peak-to-peak and RMS values, are given by the histogram statistics generated by the oscilloscope (see Fig. 2).

### 3. Measuring jitter with LVP

There are several key differences between measuring period jitter on an oscilloscope, and measuring jitter using Jitter Mitigation on an LVP tool.

First, the oscilloscope is capable of being triggered by the signal being measured itself while the LVP tool requires a separate electrical signal to generate the trigger. This difference means that LVP waveforms are sensitive to jitter introduced on the electrical trigger signal path as well as to jitter introduced on the signal path of interest. To separate the two contributions, the jitter on the trigger signal path itself can be first characterized by LVP probing. This limitation did not impact our analysis because the signal path of interest was driving an I/O pad, which we were able to trigger on.

Second, the particular clock edge that the oscilloscope triggers on is random, so that all possible clock periods can be (eventually) captured. The LVP tool, on the other hand, requires a fixed trigger period (i.e., loop length), and, therefore, may not sample all possi-

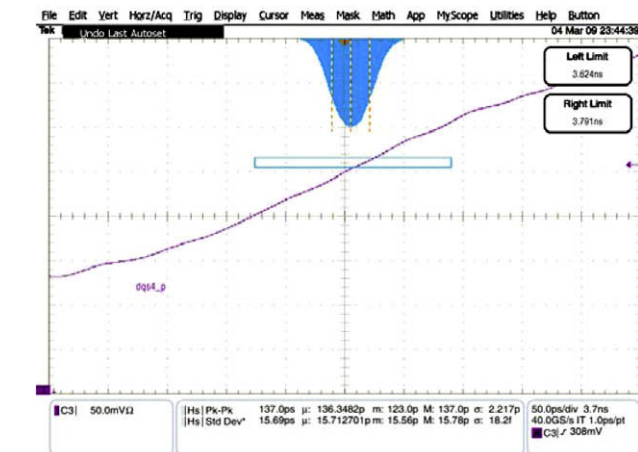


Fig. 2. Histogram measurements of a rising edge of the GPU clock signal to characterize period jitter on the device's external output. RMS (i.e., standard deviation) value of jitter is 15.7 ps. Converting to FWHM (by multiplying by 2.35 for a normal distribution) gives 37 ps jitter.

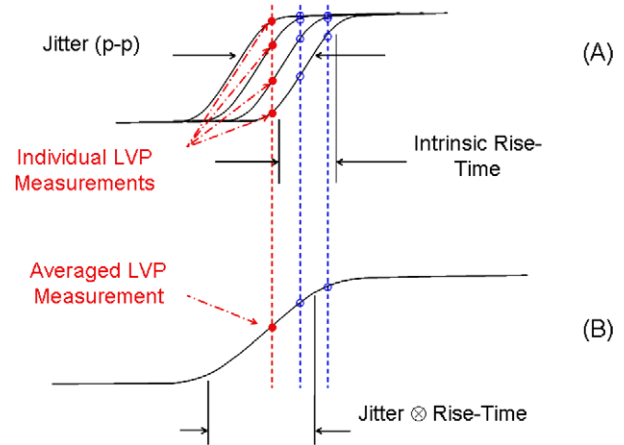


Fig. 3. Diagram illustrating how jitter convolves with signal rise-time in LVP waveforms due to averaging: (A) shows a jittery edge that is sampled by the LVP tool over multiple repetitions of the signal and (B) shows the resultant LVP waveform in which each point is generated by averaging the individual measurements. LVP measured rise-time is degraded by the jitter.

ble clock periods. Thus, the LVP jitter measurement may not give the true extent of jitter in the signal. This limitation did not impact our analysis because our approach did not require measuring the true extent of jitter, only the relative jitter difference between two modes of chip operation.

Finally, a single LVP measurement has signal-to-noise ratio (SNR)  $\ll 1$  (which is why the LVP tool can not be directly triggered by the signal being measured) so single-shot LVP waveform captures are not possible. To achieve a useful SNR in the final LVP waveform, many individual measurements must be averaged together. Unfortunately, averaging prevents jitter from being directly detected in the LVP waveforms: jitter is convolved with the measured rise/fall time of the node being probed and can only be detected through its effect on waveform rise/fall times (see Figs. 3 and 6).

Several factors influence the measured rise/fall time of the LVP waveforms: (1) The intrinsic rise or fall time of the node,  $t_{switch}$ ; (2) the step response time of the LVP tool,  $t_{lvp}$  ( $=0.35/BW$ , where  $BW$  is the tool bandwidth); and (3) jitter, including PLL jitter and any excess jitter caused by signal cross-talk, etc.:  $J_{PLL}$  and  $J_{Excess}$ .

All of these components convolve together to give the rise/fall time of the acquired LVP waveform. Assuming Gaussian response for all components (random jitter, Gaussian frequency response of the LVP system, and Gaussian-integral edge profile<sup>1</sup>), the rise/fall time,  $t_{R/F}$ , of the acquired waveform is given by adding all of the contributions in quadrature:

$$t_{R/T} = \sqrt{(t_{LVP})^2 + (t_{switch})^2 + (J_{PLL})^2 + (J_{Excess})^2} \quad (1)$$

where  $J_{PLL}$  and  $J_{Excess}$  are FWHM measurements of the corresponding jitter distribution, and all rise/fall time measurements are 20–80% values.<sup>2</sup> Since all of these factors convolve together to affect the measured rise/fall time, detecting a small amount of excess jitter requires reducing the contributions from all other factors as much as

<sup>1</sup> That is, the edge is assumed to be modeled using an error function,  $erf(x)$ . In practice, edges are fitted to a hyperbolic tangent function,  $tanh(x)$ , using the LVP tool. Assumption of an  $erf(x)$  fit is justified here since the differences are minor in the context of this discussion.

<sup>2</sup> More properly, the rise-times should be measured from 24% to 76% points to match the FWHM measurements of the other factors. However, 20–80% rise/fall time measurements are more common, and the error in using 20–80% values is  $<10\%$ , which is not significant in the context of the discussion.

possible; hence the importance of having a high-bandwidth LVP tool (to minimize  $t_{LVP}$ ) and Jitter Mitigation (to eliminate  $J_{PLL}$ ).

The following simple estimates, based on the application of Eq. (1), demonstrate the importance of eliminating the contributions of PLL jitter for detecting small amounts of excess jitter. Assuming  $t_{VP} = 20$  ps (17.5 GHz),  $t_{Switch} = 40$  ps, and  $J_{PLL} = 100$  ps, and using  $J_{Excess} = 39$  ps (obtained from the electrical measurements):

(A) For the case of no Jitter Mitigation:

$$t_{R/T}(\text{idle}) = \sqrt{(20)^2 + (40)^2 + (100)^2 + (0)^2} = 110 \text{ ps} \quad (2)$$

and

$$t_{R/T}(\text{stress}) = \sqrt{(20)^2 + (40)^2 + (100)^2 + (39)^2} = 116 \text{ ps} \quad (3)$$

for idle and stressed conditions, respectively. This represents a 3.5% change in measured rise/fall time, which is extremely difficult to reliably discern with LVP.

(B) With Jitter Mitigation:

$$t_{R/T}(\text{idle}) = \sqrt{(20)^2 + (40)^2 + (0)^2 + (0)^2} = 45 \text{ ps} \quad (4)$$

and

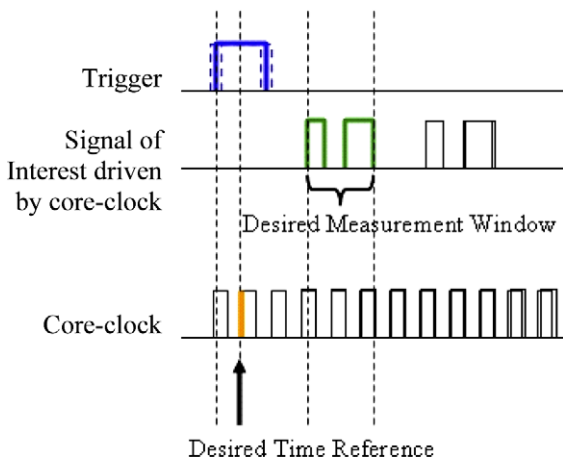
$$t_{R/T}(\text{stress}) = \sqrt{(20)^2 + (40)^2 + (0)^2 + (39)^2} = 59 \text{ ps} \quad (5)$$

for idle and stressed conditions, respectively. This gives a 28% difference in measured rise/fall time. This magnitude difference is much more reliably discerned which, again, demonstrates the importance of eliminating the effects of PLL jitter for our analysis.

#### 4. Jitter Mitigation

Details of the Jitter Mitigation features implemented in the latest LVP tool have been previously reported [1]. Here we only provide an overview. Jitter Mitigation requires both an electrical clock timing reference of interest (for example, the output of the internal PLL) and the normal trigger signal that is generated or derived from the DUT stimulus. The Jitter Mitigation circuitry of the LVP tool uses the normal trigger signal to ‘qualify’ or select a single edge of clock timing reference. (we refer to selected clock edge as the “qualified clock edge,” or QCE).

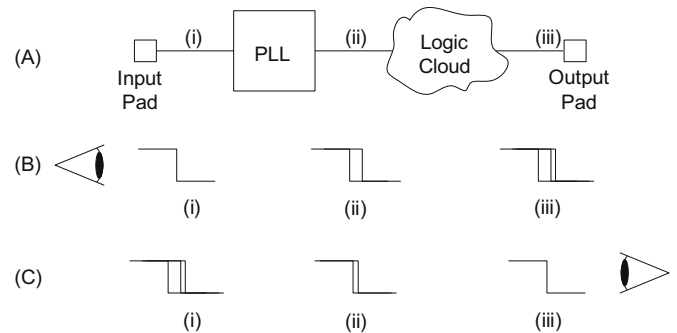
Fig. 4 is a timing diagram showing how the QCE is selected using the Jitter Mitigation electronics, and how it is used to reduce



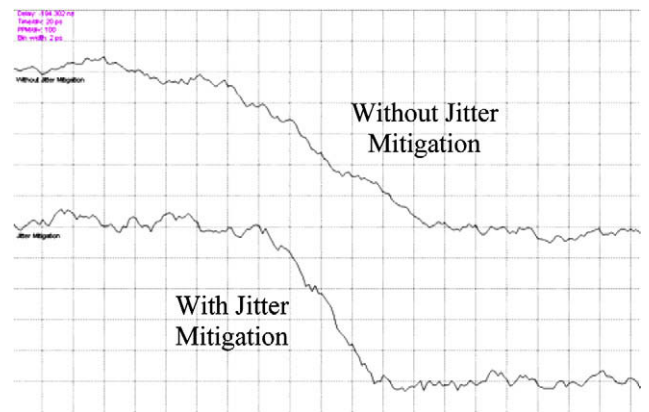
**Fig. 4.** Timing diagram illustrating Jitter Mitigation operation. All timing is shown relative to the QCE (arrow). The normal trigger (top) is used to select, or qualify, an edge (arrow) of the core-clock from the PLL for use as the timing reference for the measurements. Jitter in the signal of interest in the core-clock domain is removed from the measurements if it is coherent with the jitter of the QCE.

jitter. For clarity, signals are shown from the vantage of the QCE (that is, the QCE is assumed to be fixed in time while everything else jitters relative to it). The on-chip PLL introduces jitter between the normal trigger (top) which is generated by the DUT stimulus, and the core-clock from the PLL (bottom). Any signal of interest (middle) in the core-clock domain has jitter that is synchronized with the jitter in the PLL clock and any following logic. The Jitter Mitigation electronics uses the normal trigger signal to qualify an edge of the core-clock (arrow) to use as the time reference for the measurement, instead of using the normal trigger itself. Jitter in the signal of interest that is synchronized with the jitter of the QCE is, therefore, removed from the measurement.

Fig. 5 illustrates how Jitter Mitigation can be applied to help localize subtle sources of jitter by eliminating PLL jitter. Fig. 5A is a block diagram of the clock path from its source at the input pad, through the PLL and logic cloud, to its output pad. The PLL and the logic cloud both inject jitter into the clock signal. Fig. 5B shows how, from the vantage point of the stable reference clock signal at the input pad, the excess jitter injected by the logic cloud



**Fig. 5.** (A) Block diagram of clock signal path from input to output. Jitter is injected into the signal by the PLL, as well as by the activity in the logic cloud. (B) Falling edge of clock signal at different points in the clock signal path, from the perspective of an observer in the clock domain of the stimulus. (i), (ii), and (iii) represent a falling edge at the corresponding points in the signal path in (A). From this vantage, jitter in the falling edge increases from (i) to (iii). The excess jitter introduced by the logic cloud is small relative to the total jitter, which is dominated by the PLL. (C) Falling edge of clock signals from the perspective of an observer in the output clock domain. From this vantage, jitter increases from (iii) to (i). The small amount of excess jitter injected by the logic cloud now represents a relatively large change in total jitter, which is easier to detect.



**Fig. 6.** Example of LVP waveforms taken without Jitter Mitigation (top) and with Jitter Mitigation (bottom). Rise times, measured between the 20% and 80% points of each waveform, are 95 ps and 39 ps, respectively. These waveforms clearly demonstrate the effectiveness of Jitter Mitigation for reducing jitter in the measurements.

is masked by the much greater PLL jitter. Fig. 5C shows how this excess jitter is more easily detected when taking the vantage point of the output clock signal. Jitter Mitigation provided us with a means to realize the situation illustrated in Fig. 5C.

Fig. 6 shows an example of LVP waveforms acquired using the normal trigger (i.e., without Jitter Mitigation) versus using the QCE (i.e., with Jitter Mitigation) as the timing reference. Without Jitter Mitigation, the measured rise-time is 95 ps, while it is 39 ps with Jitter Mitigation. Absent other sources of jitter, the PLL jitter can be estimated using Eq. (1):

(A) For the LVP measured fall time without jitter mitigation:

$$t_{R/T} = \sqrt{(t_{LVP})^2 + (t_{Switch})^2 + (J_{PLL})^2} = 95 \text{ ps} \quad (6)$$

(B) For the LVP measured fall time with jitter mitigation:

$$t_{R/T} = \sqrt{(t_{LVP})^2 + (t_{Switch})^2} = 39 \text{ ps} \quad (7)$$

solving these for the PLL jitter gives  $J_{PLL} = 87$  ps, close to our 100 ps estimate above.

## 5. Approach to analysis

The focus of this analysis was to localize the source(s) of excess jitter being introduced into the PLL's core-clock signal path when the GPU was electrically stressed. One possible approach was to acquire LVP waveforms at each point of interest along the clock path, and then attempt to extract the excess jitter using Eq. (1). However, this approach requires information about the intrinsic switching time of the node being probed.

Since the excess jitter was not present when the GPU was in idle mode, an alternate approach could be taken: waveforms at the nodes of interest were measured in stress and in idle modes, and their rise-times compared. Nodes along the whole clock signal path between PLL and I/O pad were probed. A sudden change in rise/fall time difference between stress and idle modes indicated a location where excess jitter was introduced. This second approach allowed the analysis to proceed even with limited circuit design and simulation information.

The core-clock signal used for Jitter Mitigation was accessed at the I/O pad where the preliminary electrical jitter analysis was performed. This resulted in a setup similar to the one depicted in Fig. 5C. As illustrated in Fig. 5C, using this setup, jitter was expected to increase as probing progressed backwards towards the PLL from the I/O pad.

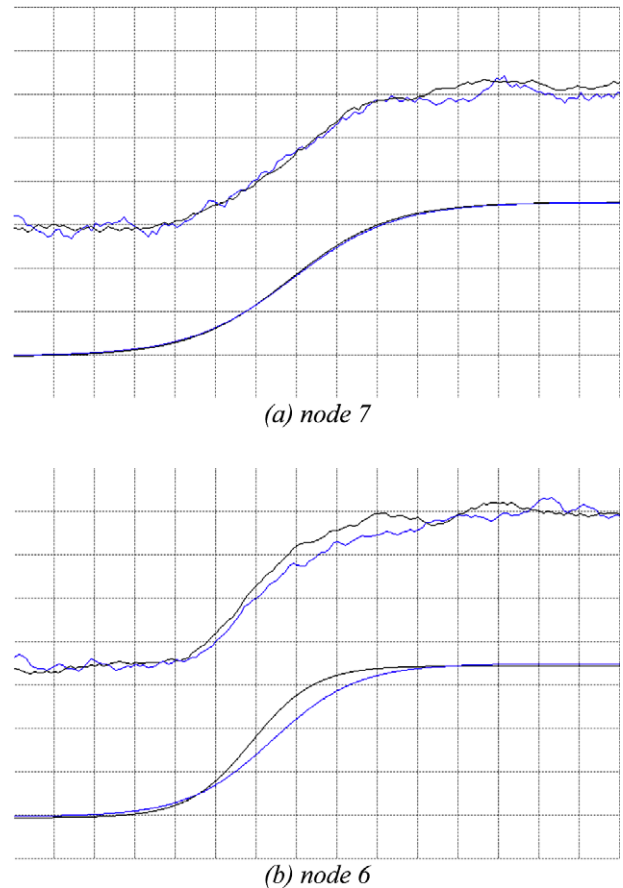
## 6. Results

Table 1 lists the rise-time measurements and differences on each node as the PLL core-clock propagates from the PLL to the

**Table 1**

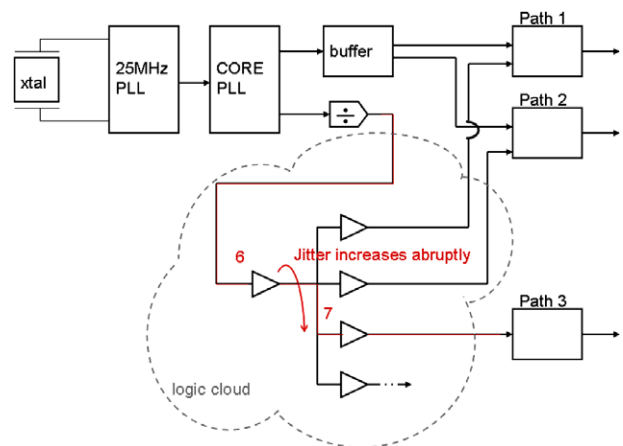
Summary of LVP rise/fall time measurement results in both idle and full-stress operating modes. Rise/fall time values were averaged over five or more separate measurements.

Node	Rise-time idle (ps)	Rise-time stressed (ps)	Rise-time difference (ps)
1	43.0	60.4	17.4
2	Not probed	Not probed	–
3	33.4	44.0	10.6
4	Not probed	Not probed	–
5	Not probed	Not probed	–
6	43.4	57.4	14.0
7	71.6	74.8	3.2
8	46.4	47.3	0.9
9	74.3	76.4	2.1
10	52.3	55.3	3.0
PAD	56.4	60.4	4.0



**Fig. 7.** Acquired and fitted LVP waveforms under idle mode (black curve) and full-stressed mode (blue curve). The rise-time difference between the two modes is negligible for node 7 (a) but significant in node 6 (b). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

I/O PAD. The measurements show a sudden increase in the rise-time differences between nodes 7 and 6. Prior to node 7 (in the direction from PAD to PLL), the rise-time differences were less than 5 ps, which is statistically insignificant, based on the repeatability of the LVP measurements. After the sudden increase between

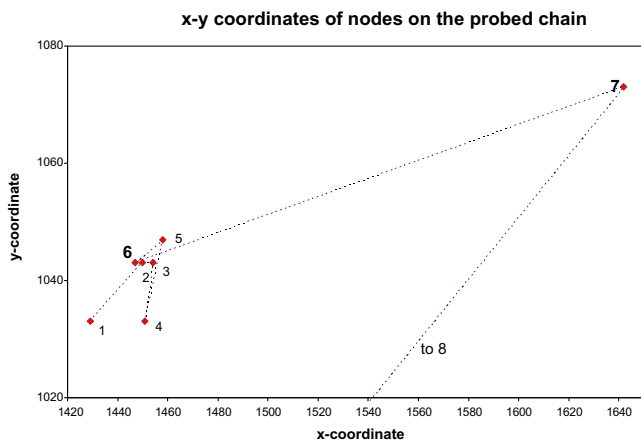


**Fig. 8.** Schematic block diagram of three signal paths with clocks generated from the same PLL. Path 3 showed excess jitter under load. LVP probing identified an abrupt jitter increase along path 3. Nodes 1–10 in Table 1 are along the red-linked path. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

**Table 2**

Buffer type and number of fan-outs for each node in the jittery path. Nodes 1, 3, 6, and 10 are of the same buffer type, but drive different numbers of fan-outs.

Node	Buffer type	Number of fan-out
1	A	2
2	B	1
3	A	4
4	C	3
5	D	1
6	A	14
7	E	1
8	E	3
9	F	1
10	A	1



**Fig. 9.** Physical location (X–Y coordinates) of the buffers (nodes) along the jittery path.

nodes 7 and 6, the rise-time differences were greater than 10 ps. This localized the source of the excess jitter to node 6.

Fig. 7 shows the LVP waveforms for nodes 7 and 6. Two pairs of waveforms are presented in each plot: the upper pair are the acquired LVP waveforms, in idle (black) and stress (blue) modes, while the lower pair are the corresponding curve fits (fitted to the hyperbolic tangent function) to the waveforms. To ensure repeatability of the LVP waveforms, multiple acquisitions were

performed and rise/fall time values for each node were averaged over five or more separate measurements.

### 7. Root cause analysis

LVP probing identified an abrupt jitter increase from node 6 to node 7 in the clock signal path of the GPU (Fig. 8). Consultation with design engineering revealed that the clock buffer at node 6 drives a larger fan-out that might be atypical for its size (Table 2, type A buffer). Furthermore, analyzing the physical locations of the buffers along the clock signal path indicated that the distance between nodes 6 and 7 is substantially longer than the distance between two consecutive nodes preceding node 6 (Fig. 9).

The excess jitter observed in this region could be due to the combination of the large number of fan-outs (loading node 6 too heavily) and the long distance between nodes 6 and 7 (increasing the chance for signal cross-talk). Design modification(s) to eliminate the excess jitter introduced at this sensitive region are currently being investigated for the next generation GPU.

### 8. Conclusions

With the development of Jitter Mitigation technology for LVP tools, jitter analysis for PLL driven circuits is not only now possible but also practical.

While characterization of absolute period jitter was possible, it was more practical in this case to compare the difference in jitter between two operating modes.

The LVP tool was utilized for this analysis as it has the required bandwidth to fulfill the need to measure tens of pico-second rise/fall times. Its superior low  $V_{dd}$  probing capabilities enabled high measurement throughput.

The design issues uncovered may seem obvious after the measurements were completed, but the fact that they slipped through the extensive design and simulation process shows both the complexity of IC design and the values of the failure analysis laboratory and their electrical diagnostics capabilities.

### References

- [1] Ng Yin S, Lo W, Wilsher K. Next generation laser voltage probing. In: Proceeding, international symposium on testing and failure analysis; 2008. p. 249.
- [2] Wilsher KR, Lo WK. Practical optical waveform probing of flip-chip CMOS devices. In: Proceedings, international test conference (ITC); 1999. p. 934.