

Scan chain debug using Dynamic Lock-In Thermography

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Abstract

In this paper, we demonstrate that lock-in thermography (LIT) appears as a key and complementary technique for Failure Analysis across different use cases. Even if the failure requires a complex emulation setup, thanks to a specific capability of our thermal system, this kind of failure can be addressed. In our FA case study, we will show that LIT is a most efficient solution to address a bridge defect located inside a complex logic area, and furthermore that LIT highlights the defect itself and not only the consequences of the defect.

Introduction

Lock-In Thermography has been established as a key technique in the failure analysis flow to address defects. The aim of this paper is to present a full case study related to a scan chain stuck-at failure, where the EDA diagnosis tool was not successful. Since common failure analysis methods, such as emission microscopy [1] or laser stimulation techniques [2] were not efficient enough to highlight the X-Y location of the failure and thus determine root cause. We demonstrated that Dynamic Lock-In Thermography is able to pinpoint a bridging resistance between 2 internal signal lines inside the logic section of the device.

Lock-In Thermography

Lock-In Thermography (LIT) was introduced a few years ago to overcome the limitations of the MCT thermal camera and Liquid Crystal (LC), which have been used to localize thermally active defects in microelectronic devices. The three main benefits of LIT over previous static thermal detection are:

1. Sensitivity: due to latest generation of the highly sensitive InSb camera, and the specific lock-in methodology to drastically improve the fault detection efficiency (μW range) [3]
2. Resolution: due to an advanced optical Solid Immersion Lens which open the door to sub-micron resolution in the thermal domain [4]
3. Ease of use.

The most common usage of LIT is V_{dd} -GND short localization. In this configuration, we connected the failing pins of the Device under Test (DUT) to the Lock-In thermography system, which activated (voltage \Rightarrow Vdd) and deactivated (voltage \Rightarrow GND) them at a given frequency. Then, the system applied the lock-in method based on the same known frequency on resulting infrared images. This lock-in process is applied to each pixel of the thermal detector in real time (Figure 1).

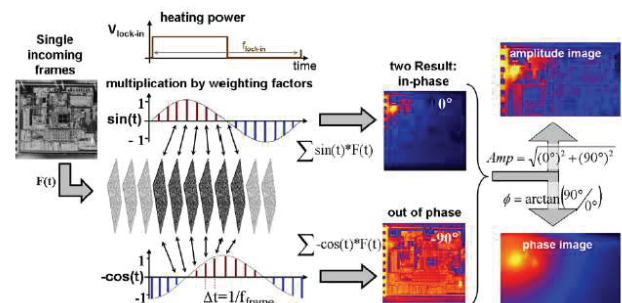


Figure 1: Basic setup of Lock-In thermography application.

This lock-in based approach is commonly used to detect and measure a very small AC signal when this signal is obscured by noise. The Signal to Noise Ratio (SNR) of the resulting lock-in thermography image improves with the acquisition time $\{\text{SNR} \propto \ln(t_{\text{acquisition}})\}$.

Dynamic Lock-In Thermography

In this paper, the LIT technique is used in a dynamic environment [5] because of the failure type. In fact, this defect cannot be activated with a simple “2 wires connection” Vdd-GND. It was detected during the scan chain test, using a dynamic ATE to activate it, and which classified it as a broken scan chain.

To amend the LIT method to this specific case study configuration (dynamic emulation needed), we built a specific test setup adapted to the lock-in thermography technique. As we already described, the basic idea is to be able to enable and disable the failure at a given frequency (lock-in frequency). First, we develop a specific test pattern revised to the previous need (discussed in detail hereafter). Second, to ensure correct lock-in methodology, the thermal camera frame rate needed to be synchronous with the defect activation. This was easily achieved on our system (ELITE) through external triggering of the thermal camera. Thus, using this specific capability, we sent a trigger signal, which occurs at the beginning of each test loop, to synchronize the thermal camera with our dynamic defect activation (Figure 2).

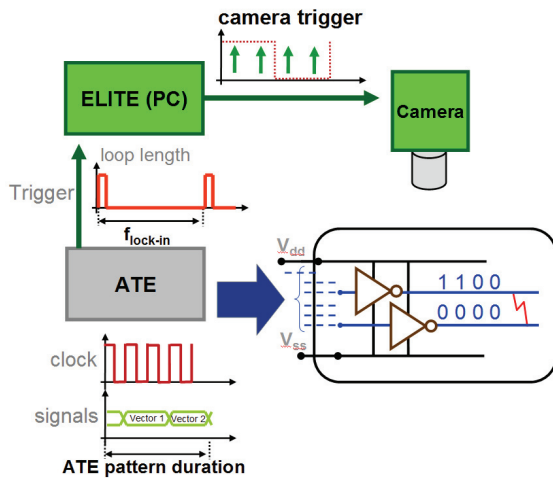


Figure 2: Dynamic Lock-In Thermography.

Failure description

This work has been performed on a 0.15 μm process device, designed for Digital TV applications, packaged in SBGA 256. The device failed during the scan chain integrity test. During this first level of test, the scan chain is setup in “serial mode” and exercised as a simple serial register. We send a known data stream in the first flip flop of the serial register (SCAN IN) and we expect to detect the same data stream at the output of the last flip flop (SCAN OUT). In our case, the SCAN OUT information was always stuck at ‘1’ and the EDA diagnosis tool did not give any useful prediction. It just classified this failure as a broken scan chain issue, and gave us the approximate failing flip flop.

Failure Localization

EMMI and Laser Based Approach:

The first set of acquisitions was acquired on a high performance emission tool (EMMI). Unfortunately, in this case, EMMI highlighted only defect consequences but it was not able to pinpoint the source of the defect. This is a well-known limitation of the EMMI technique, such as when dealing with a bridge defect located inside a logic area [6]. Also, Laser stimulation technique like OBIRCH [7] was tried in pseudo static mode due to electrical setup (stopping on failing vector) without a valid signature at low (1x) and mid-magnifications (20x). This can be explained by the fact that the defect had a relatively low resistance value (few tens of ohms) and its geometric dimension was small compared to the laser beam size at these magnifications. Thus, resistance change of the defect was not sufficient to induce a detectable consumption variation.

Specific Test Pattern Generation for LIT Analysis:

To analyze this device using the LIT tool, the first step is to setup specific test pattern to be adapted to the external trigger setup of the camera. This part of the process can be tricky when dealing with more complex failure activation. Let’s add that we can use various techniques to meet this electrical activation requirement.

In this case study, we used a 10MHz clock (nominal frequency), we send 25000 ‘0’ followed by 25000 ‘1’. At the same time, in the beginning of each test loop we generated a trigger signal to the system using a dedicated output of the ATE. As a result, the failure is ‘activated’ during the first half of the test pattern, and ‘not activated’ during the second part of the test pattern (Figure 3).

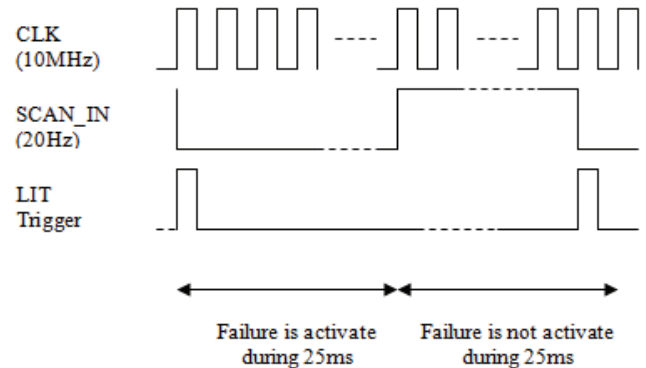


Figure 3: Simplify test pattern used for the LIT analysis.

Lock-In Thermography Analysis:

As a common defect localization approach, the first step was to analyze the entire failing die at a low magnification (1x \leftrightarrow Field Of View = 9.6mm x 7.68mm). Figure 4 shows 1x LIT images, performed on a golden device and on the failing device.

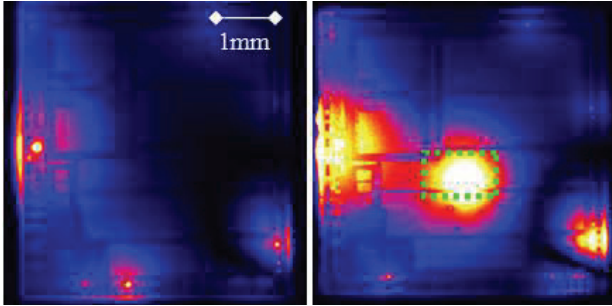


Figure 4: LIT amplitude images from a golden device (left) and a failing device (right). LIT frequency 20Hz. Mag.: 1x. Acq. time: ~1min.

We note that a huge thermal spot is localized, in the center of the failing die, inside the logic area. Using additional information on the chip design, the area was spatially correlated with the failing scan chain. Moreover, we can add that the golden device image was not mandatory in this case, since it was obvious that this thermal spot was coming from the failing circuit.

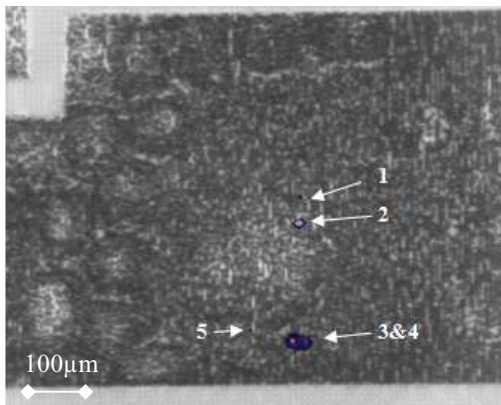


Figure 5: LIT amplitude image (superimposed on pattern image of the DUT) from the failing device (dotted box area in Figure 4). LIT frequency 20Hz. Mag.: 10x. Acq. time: ~1min.

Figure 5 shows a zoomed in 10x acquisition done on the failing device, in the logic area, where the defective thermal signature was found using the low magnification lens. We can resolve at least 5 thermal spots which were linked to the defect, since they were only visible on the failing die. One more point, these thermal spots seemed really interesting since they are spatially located near the failing scan chain implementation.

Next step was to get higher magnifications using a Thermal Solid Immersion Lens [4]. Related images are presented in Figure 6.

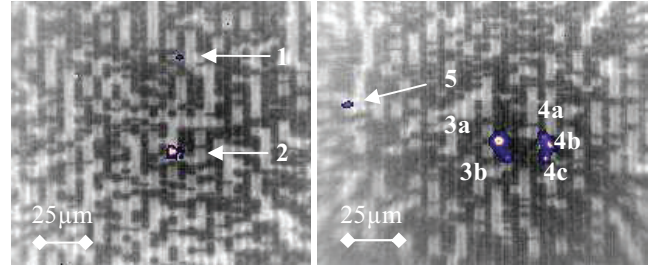


Figure 6: LIT amplitude (overlaid on pattern image) images performed on the failing device (cropped). LIT frequency 20Hz. Mag.: 17x (SIL). Acq. time: ~2min.

These high resolution images allow easy alignment to CAD information to identify which cells and nets are implicated in the failure mechanism (Figure 6). Physical Net Trace [8] analysis was performed using the CAD database.

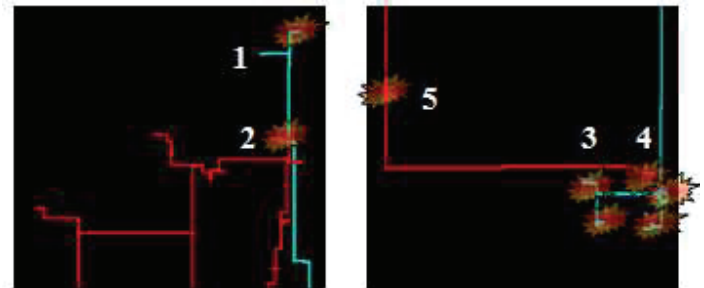


Figure 7: NetTrace results of CAD analysis

Interpretation

As we see in Figures 6 and 7, all thermal spots can be linked to two different nets (blue net for spots 1,3a, 3b, 4b and 4c; red net for spots 2, 4a and 5). Also, through this analysis we notice that all spots are spatially correlated with standard cell locations, except spot 2. Figure 8 shows a high magnification (30x) view of spots 1 and 2:

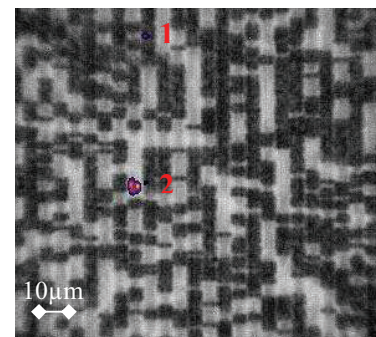


Figure 8: LIT amplitude image (superimposed on pattern image) for the failing device. LIT frequency 20Hz. Mag.: 30x (SIL). Acq. time: ~2min.

We note from this high magnification image analysis that spot 2 is not located over standard cell area (\Leftrightarrow black area), and the CAD analysis shows that this specific location corresponds to an area where the two suspect nets are in close proximity (Figure 9).

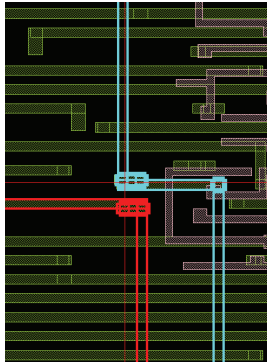


Figure 9: Closer view of CAD at the thermal spot 2 location showing the close proximity of M3 to M2 via connection.

All information collected during this analysis (test, fault localization, CAD analysis and schematic analysis) converged to a resistive bridging defect at the spot 2 location, between the two nets which are highlighted by the LIT analysis.

All other thermal spots which are present on Figure 5 can now be explained through this fail hypothesis. In fact, this resistive bridge would induce an incorrect voltage state of the two highlighted nets. Consequently, cells that are connected to these nets must be in a wrong polarity state (for gate connected) or a wrong charging (for drivers). Consequently, additional currents would have passed through these cells and heated them up. That is why we observed thermal spots on gates linked to the bridge defect.

This hypothesis was confirmed using a micro-probing approach on the output of the failing flip flop (blue net). Results are described in Figure 10.

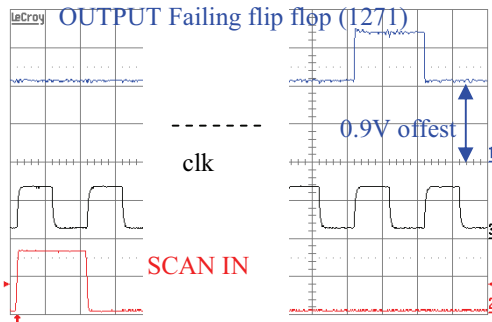


Figure 10: Oscillograph from micro-probing experiment performed on the output of the suspected flip flop.

From this experiment, we note that the lower state of the output of this flip flop is offset by 0.9V. This result is in line with a bridge defect between two nets, when the red net is set to Vdd. Moreover, we understand why this scan chain was failing during the scan chain integrity test, since this failure will result in a stuck at '1' test result on the output of this scan chain.

We severed this net to disconnect the two consecutive flip flops in that scan chain, and we were able to verify that these two independent sections of that particular scan chain was working as expected.

Finally, we can also explain the broken scan chain result that was obtained during first electrical testing. Hereafter, is presented the schematic representation of the failing area (Figure 11):

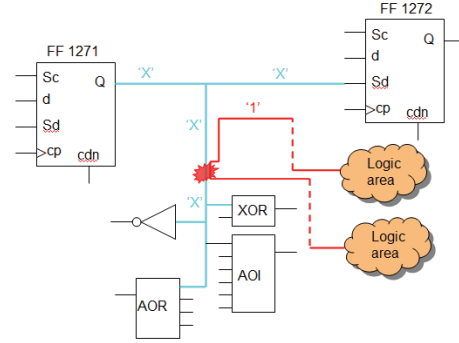


Figure 11: Schematic of the failing area of the defective scan chain.

Flip-flops used in our case study are positive edge triggered multiplexed scan D-flip-flops. The scan control input (SC) selects either the data input (D) when SC is low, or the scan data input (SD) when SC is high. The selected data is transferred to the Q output on the rising edge of the clock CP. Thus, in scan mode, since the bridge defect is located directly on the net which connects the two flip-flops of interest, it was detected as a scan chain integrity issue during the electrical test.

Physical characterization

The final step of this study was to perform a physical failure analysis at the spot 2 location to find the physical cause of the failure. Results are revealed in Figure 12:

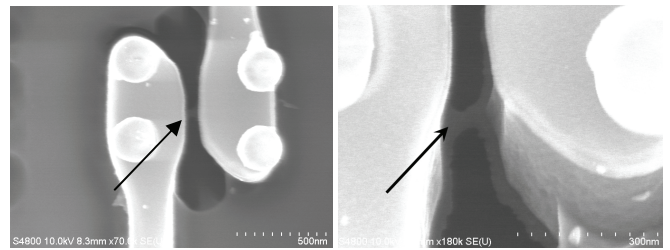


Figure 12: SEM, top view images shows barrier short between two M2 metal lines.

Physical analysis reveals a barrier short at the bottom of two M2 lines which induced a low resistive bridge defect. This issue was solved by design rule modification and this close proximity prohibition of M2 to M3 double vias was added to the design rules datalog (Figure 13).

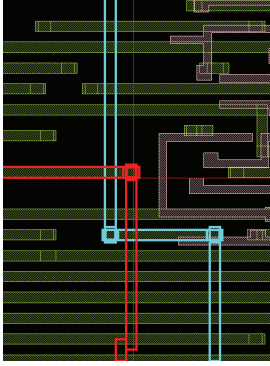


Figure 13: Closer view of CAD showing the design fix.

Conclusion

In this paper, we have addressed a successful failure analysis case study, on a dynamically activated device, using the lock-in thermography technique. We demonstrated that this thermal based technique enabled the localization of a resistive bridge inside a digital logic area, where EMMI and laser stimulation techniques were not conclusive. The main benefit is that this approach allows a direct localization of the root cause, since other classical techniques (EMMI and pseudo dynamic OBIRCH) will generally pinpoint only defect consequences.

This specific external trigger setup capability on the LIT tool opens the doors to a wide range of applications, where a defect cannot be easily emulated with a two probe setup (Vdd-GND).

Acknowledgements

All lock-in thermography experiments have been performed on CIMPACA Characterization platform. This lab is a mutualized platform between different local partners located in Rousset, France.

References

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