DCG - Seminar

Increasing the Local Operating IC Speed with Backside FIB processes

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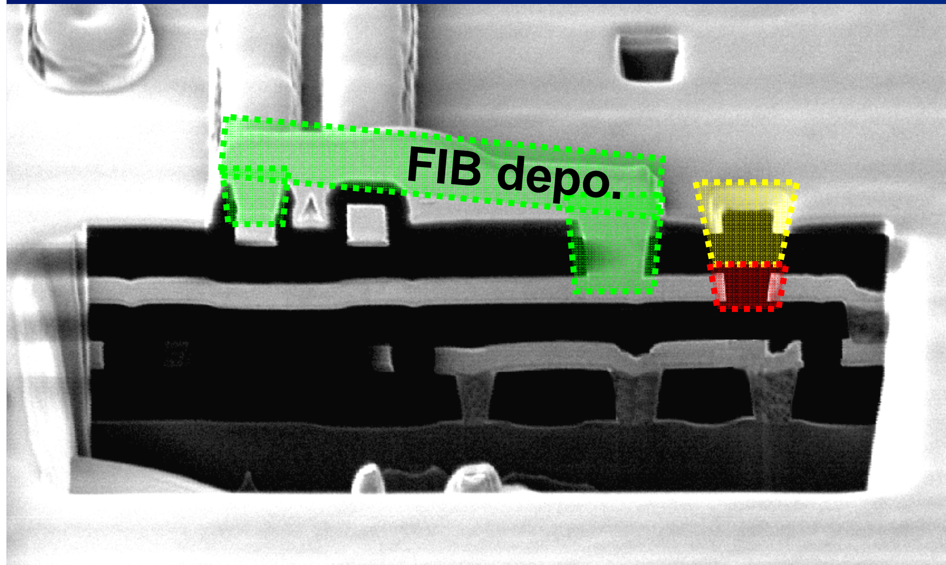
Focused Ion Beam for Circuit Edit

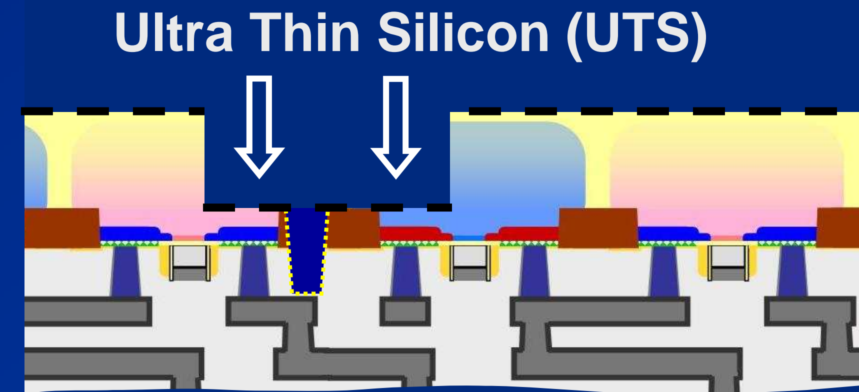
then
"frontside" CE

limited success rate due to:
- interconnect layers > 10
- most CE on lowest levels
- reduced feature size
- CMP "fill shapes"
- Packages (BGA, Flip-Chip…)

now
"backside" CE

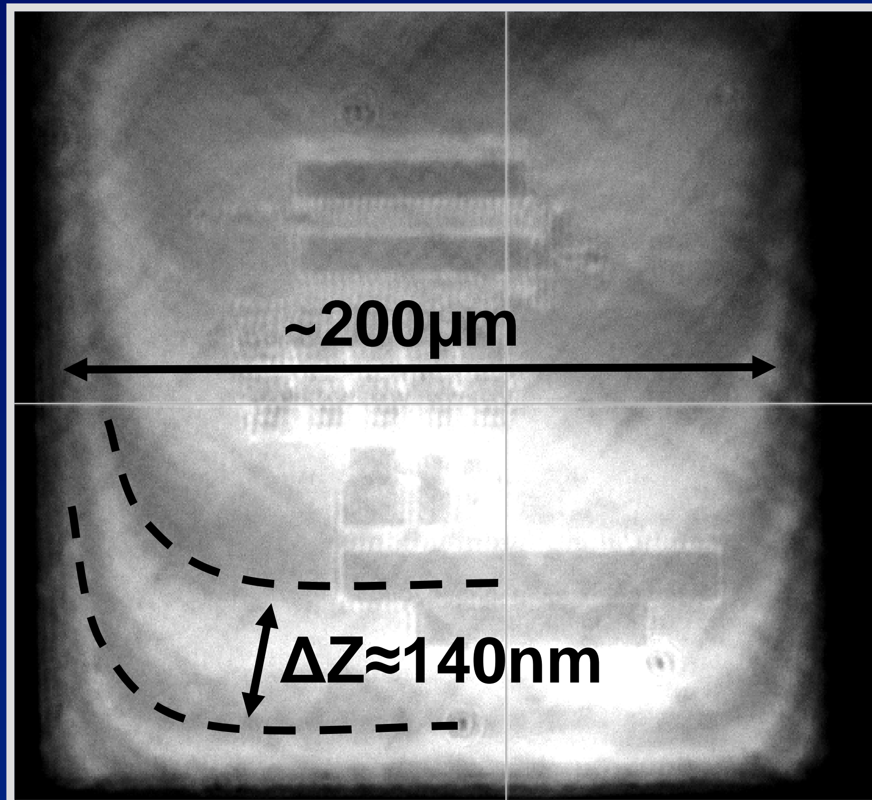
advantages:
- better access to lowest layers
- no charging problems
- highest alignment accuracy

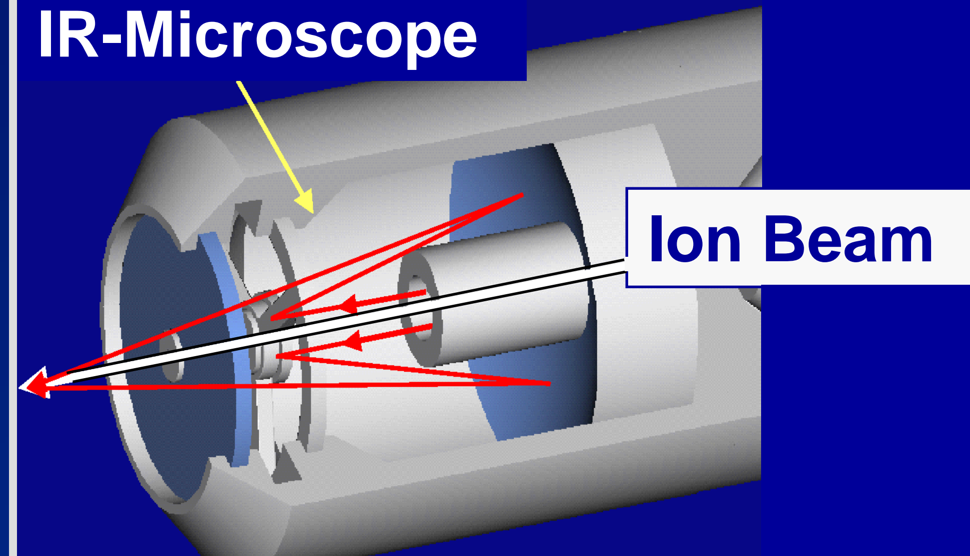




Navigation & Planarity

Through silicon navigation with co-axial IR optics





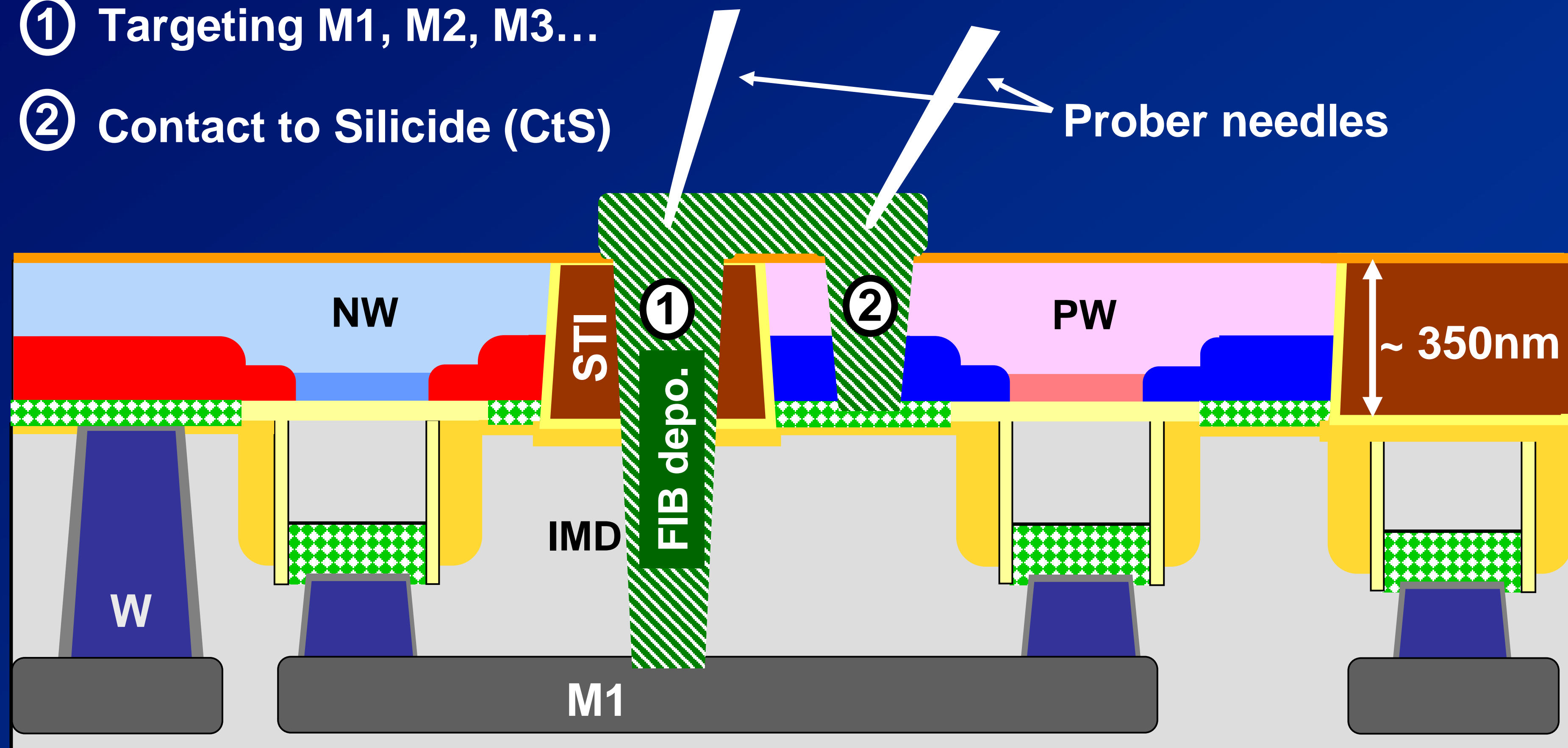
Highest Co-planarity due to optical control "on the fly"

Allows for UTS formation in wide areas

Opportunities with Ultra Thin Silicon

influence on FET performance ??

- CE with reduced Via-Resistance
- non-destructive Nano Probing (DC & RF)



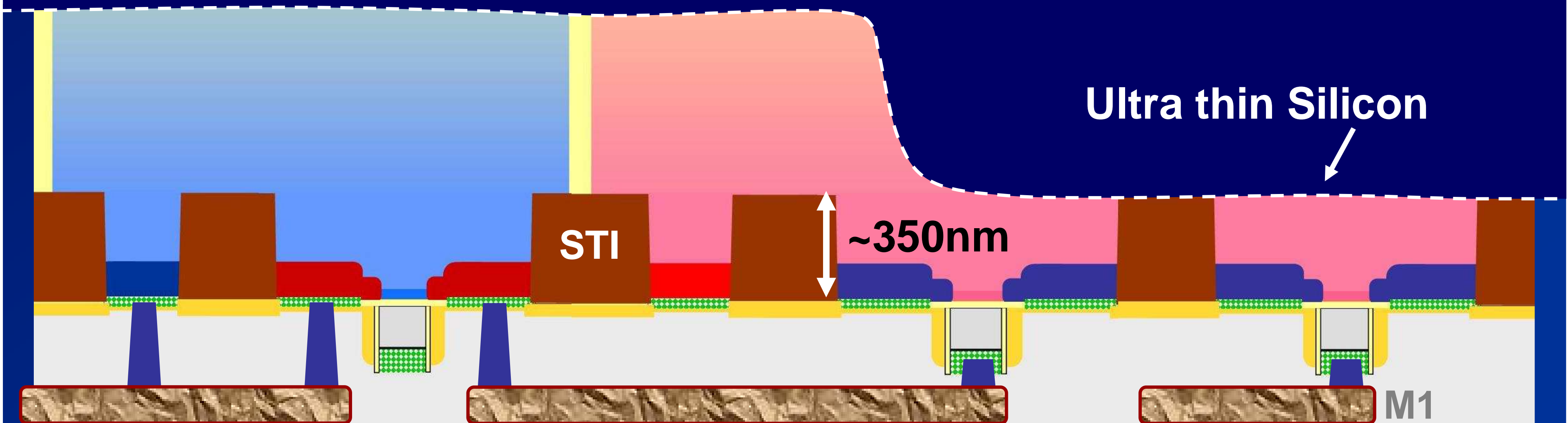
Outline

- OptiFIB trench process
- Invasiveness Study of FIB thinning

  Experimental Results DC & RF

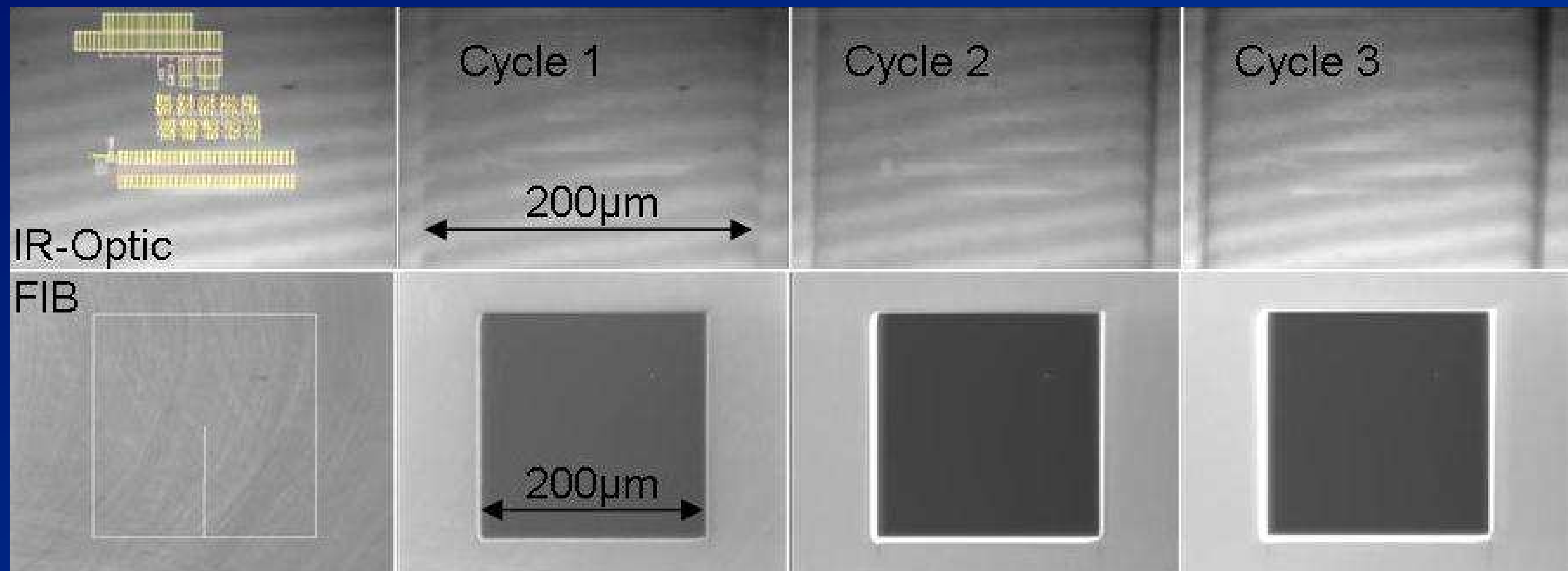
  vs.

  Simulation Results
- FIB delay trimming
- Summary



Trench to n-well level

- Sequence of pure sputtering and iodine based etch (3/1)
  - ⇨ removing residuals & flattening the surface in FOV



Trench to n-well level

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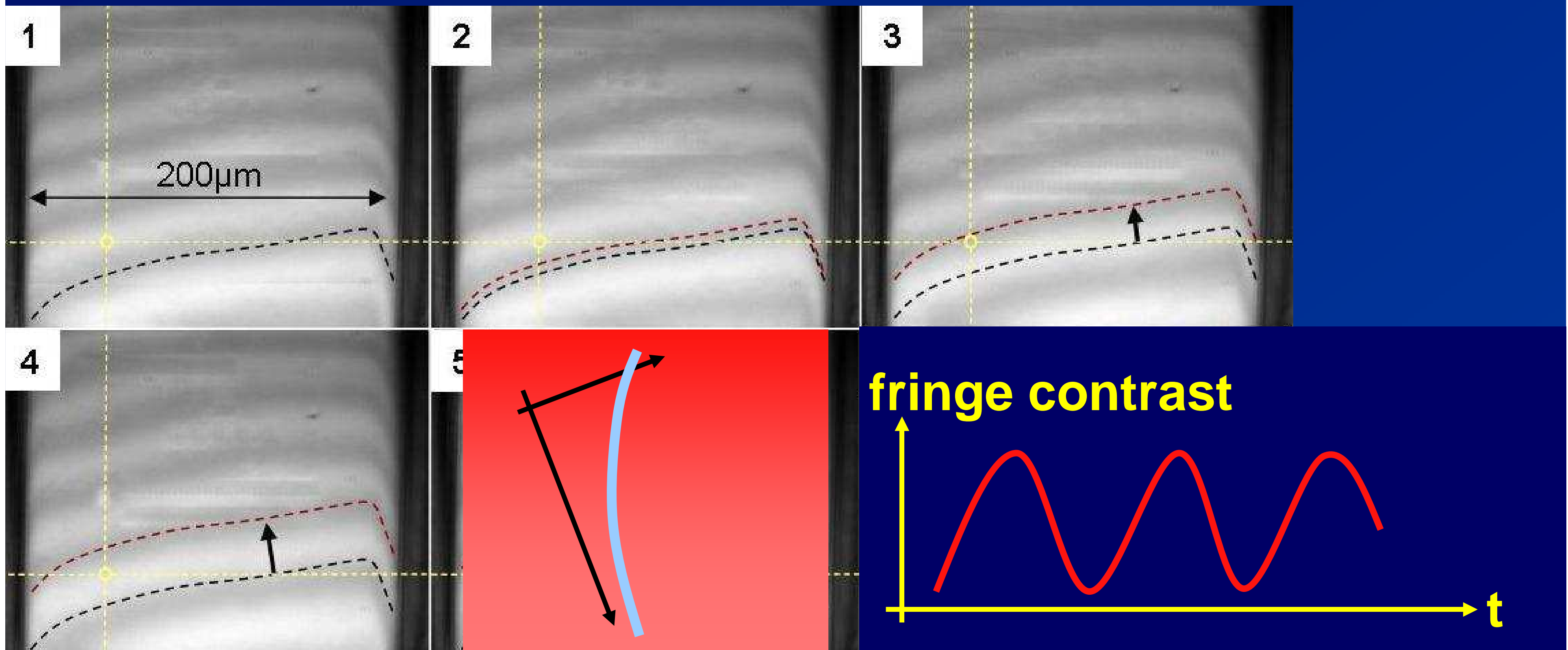
  - ⇨ removing residuals & flattening the surface
- "on the fly" co-planarity control
  - ⇨ pixel dwell time can be varied to equalize



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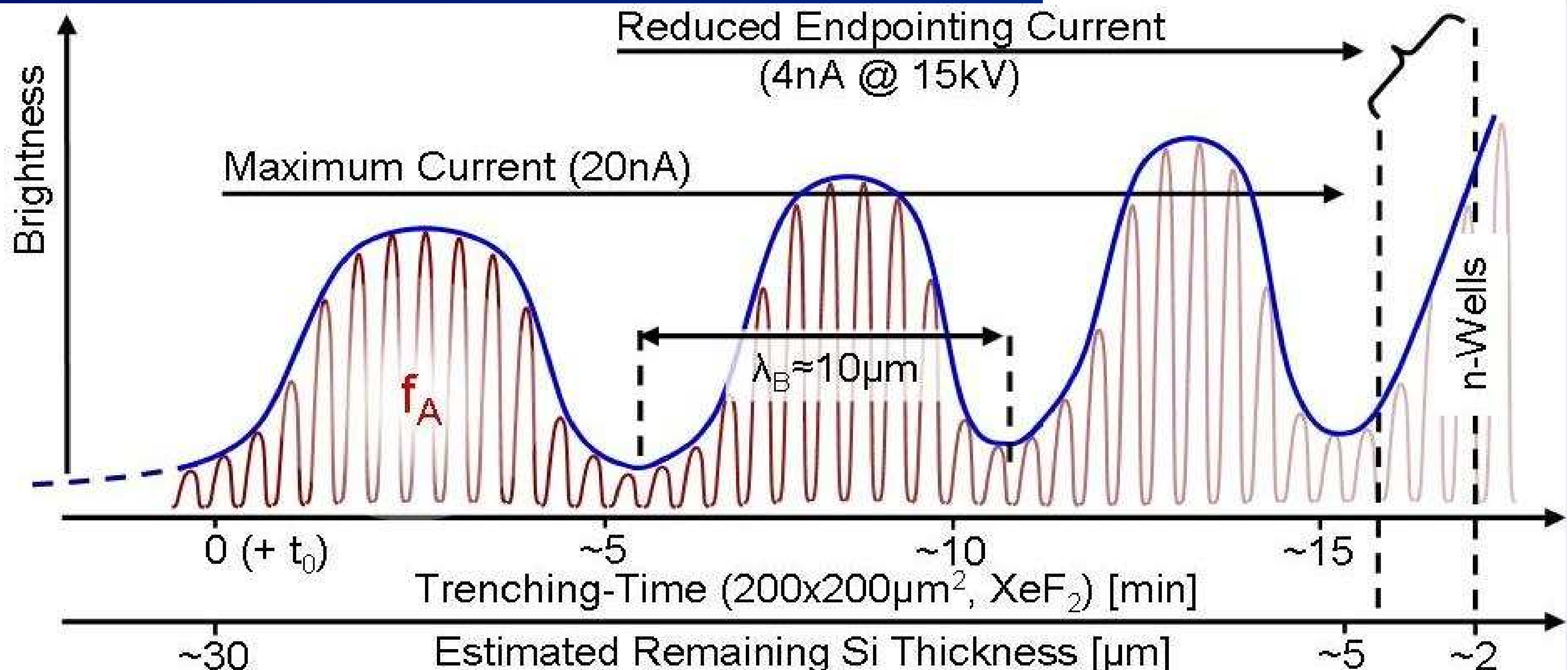
- "on the fly" thickness monitoring

better control
= faster throughput
= higher success rate



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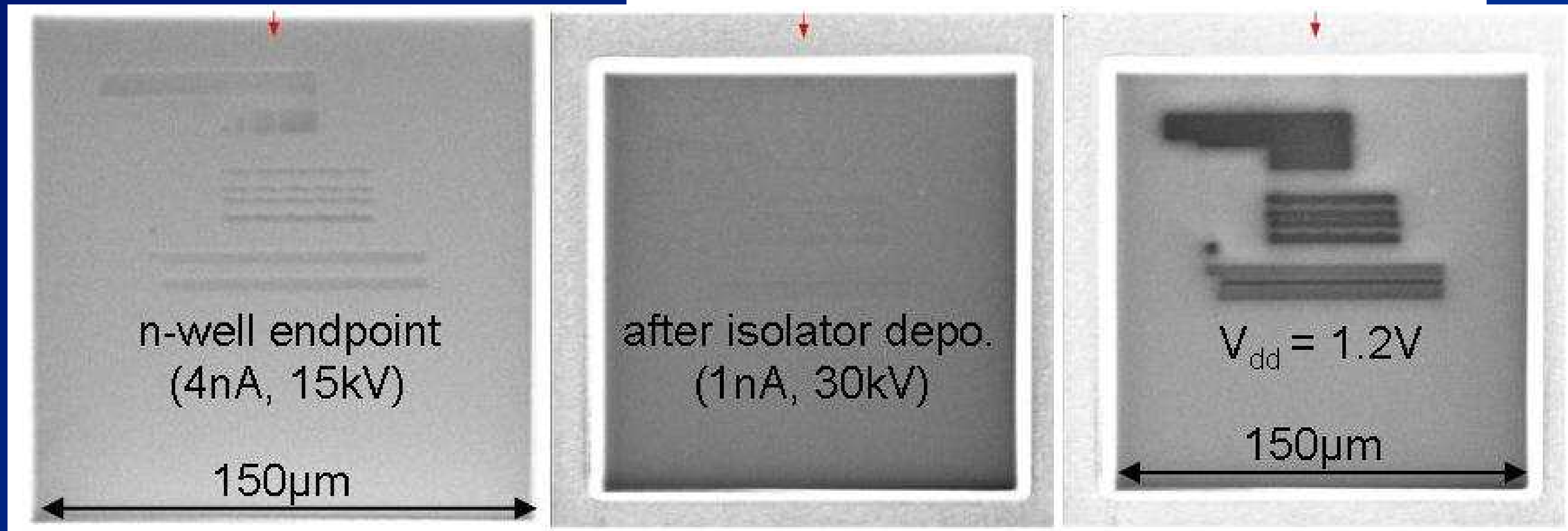
powering up the device helps !

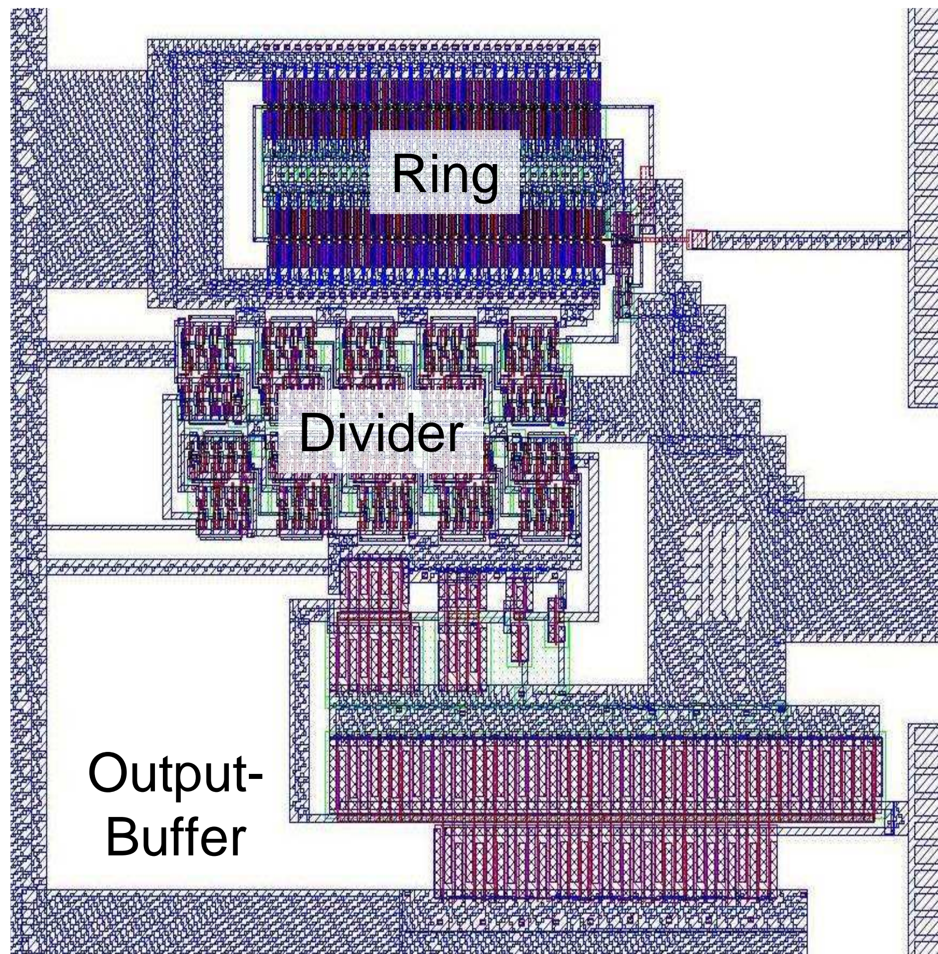


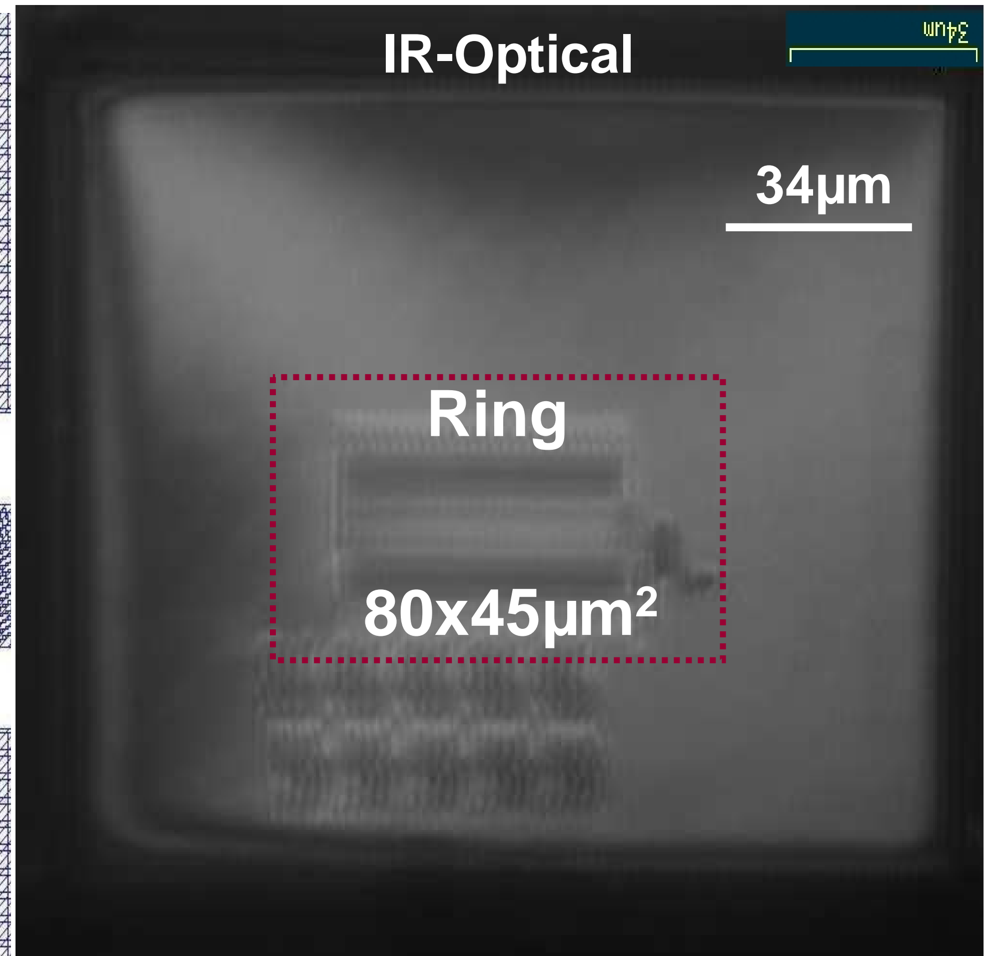
FIB thinning of DuT

n-well level (~1μm)

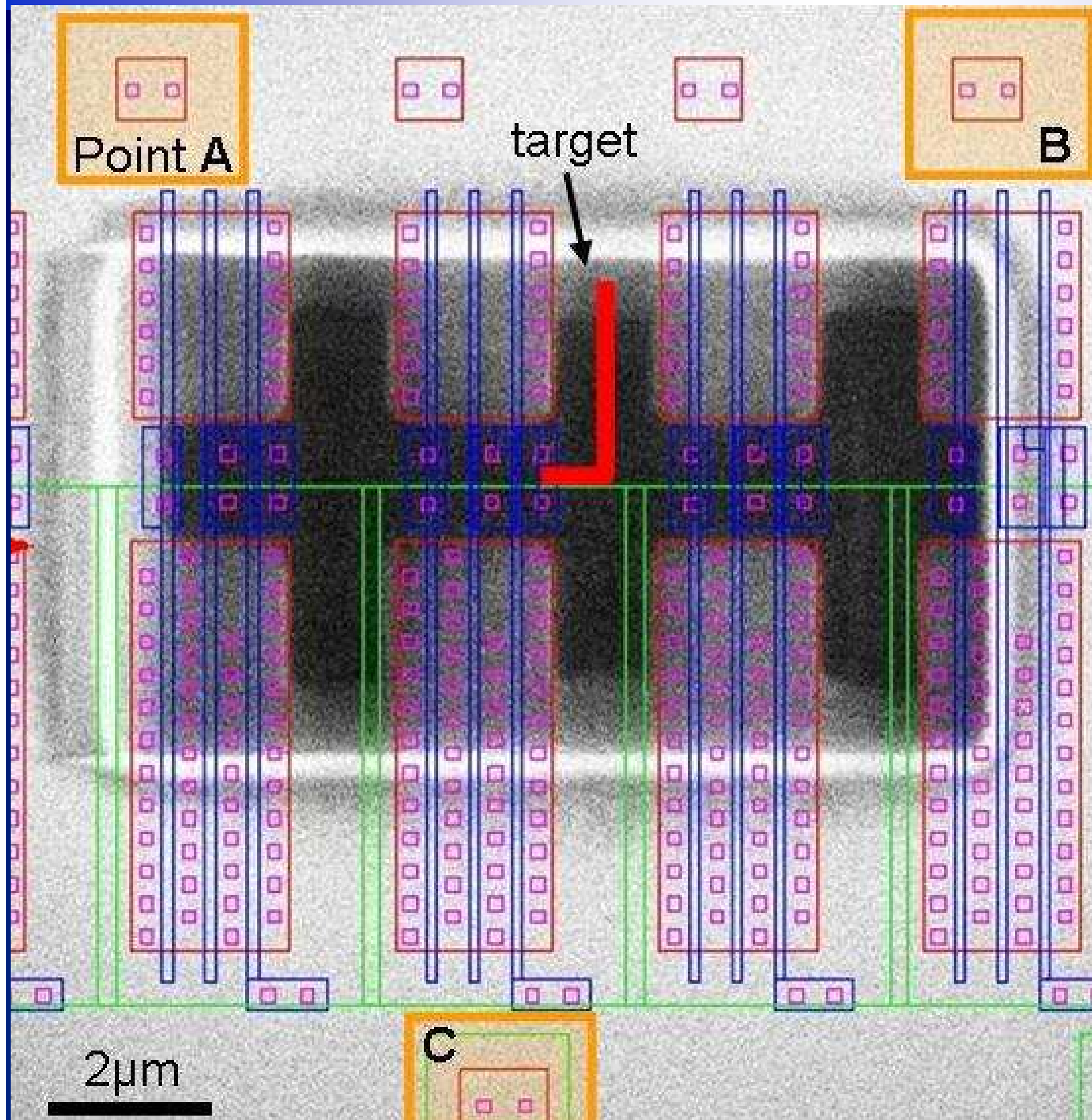
planarity mismatch < 100nm

120nm Ring Oscillator





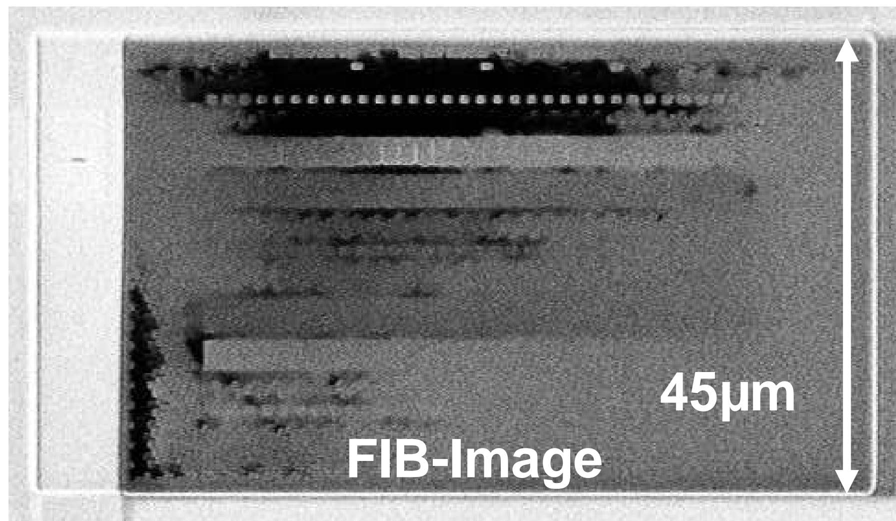
STI alignment

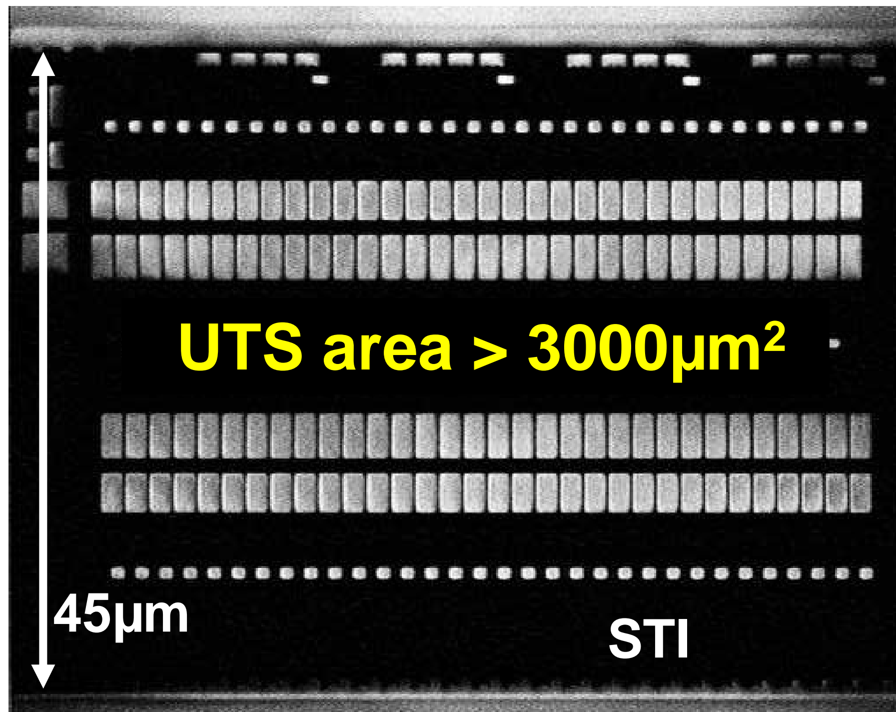


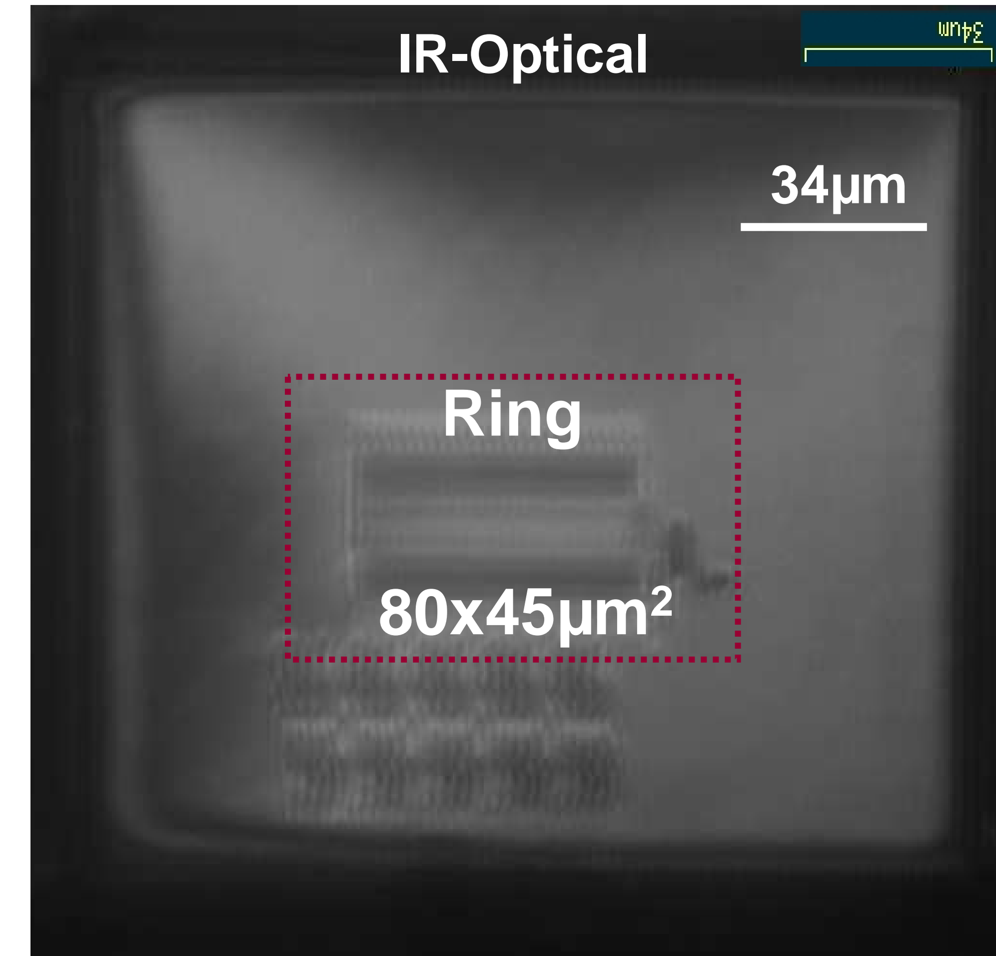
- highest possible accuracy
  ⇨ necessary
- Point A B C
  ➡ better 30nm
- local STI opening
  ➡ better ???
- FET not isolated
  ➡ no SOI effects!

evaluation of maximum effect

Impact on Circuitry Performance



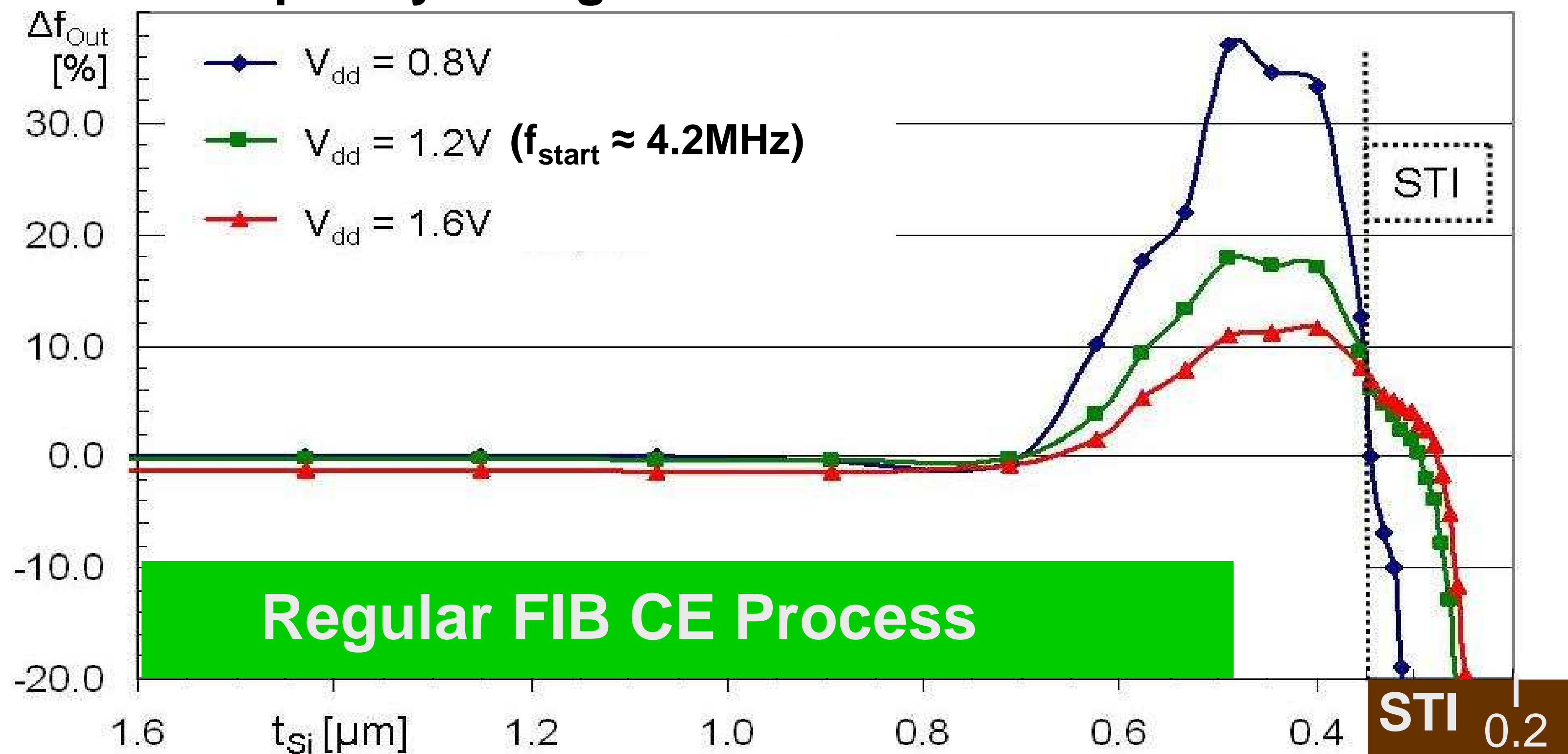




Impact on Circuitry Performance

- no effect until t_{Si} < 700nm
- ~ +20% with nominal V_{dd}
- maximum of +38% with V_{dd} = 0.8V

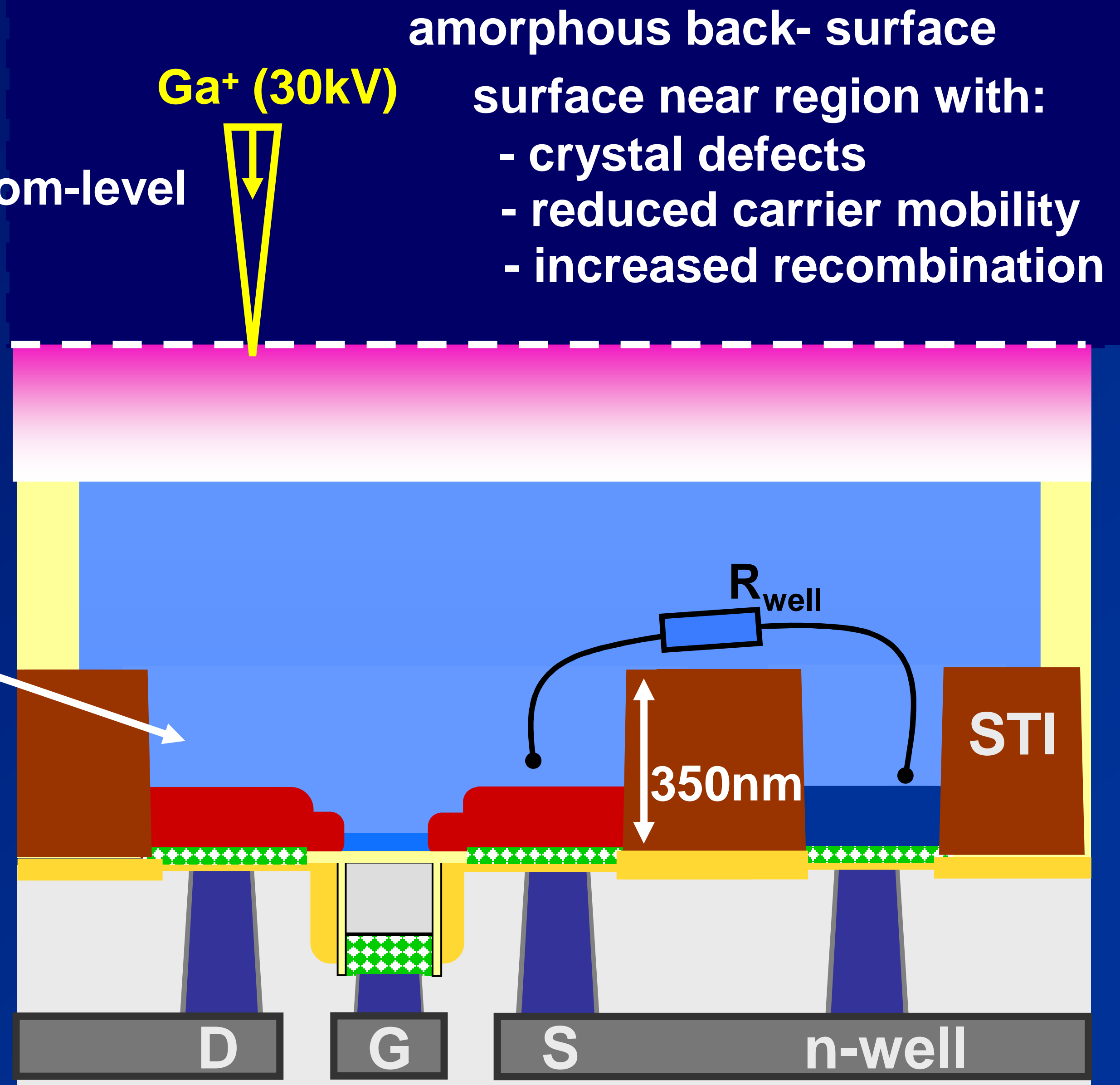
frequency change in % as a function of Si thickness



Influence of FIB Thinning

- Mechanical thinning
  50 - 10µm
- FIB thinning to well-bottom-level
  3 - 1.5µm
  increased selfheating
- FIB thinning to STI-level
  1.5 - 0.6µm

  $R_{well} \rightarrow M\Omega$
  "floating" body



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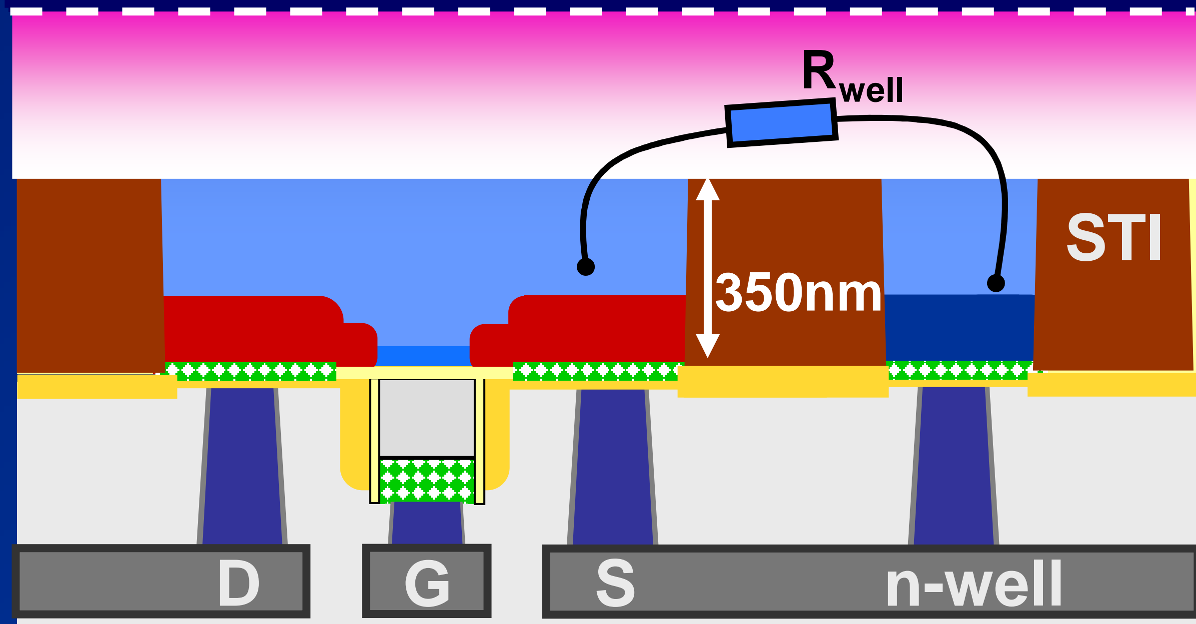
  $R_{well} \rightarrow M\Omega$
  "floating" body

  0.6 - 0.35µm
  $R_{well} \rightarrow G\Omega$
  defects in D/S SCR

- thinning below STI-level
  > 350nm
  degradation of channel mobility

amorphous back- surface

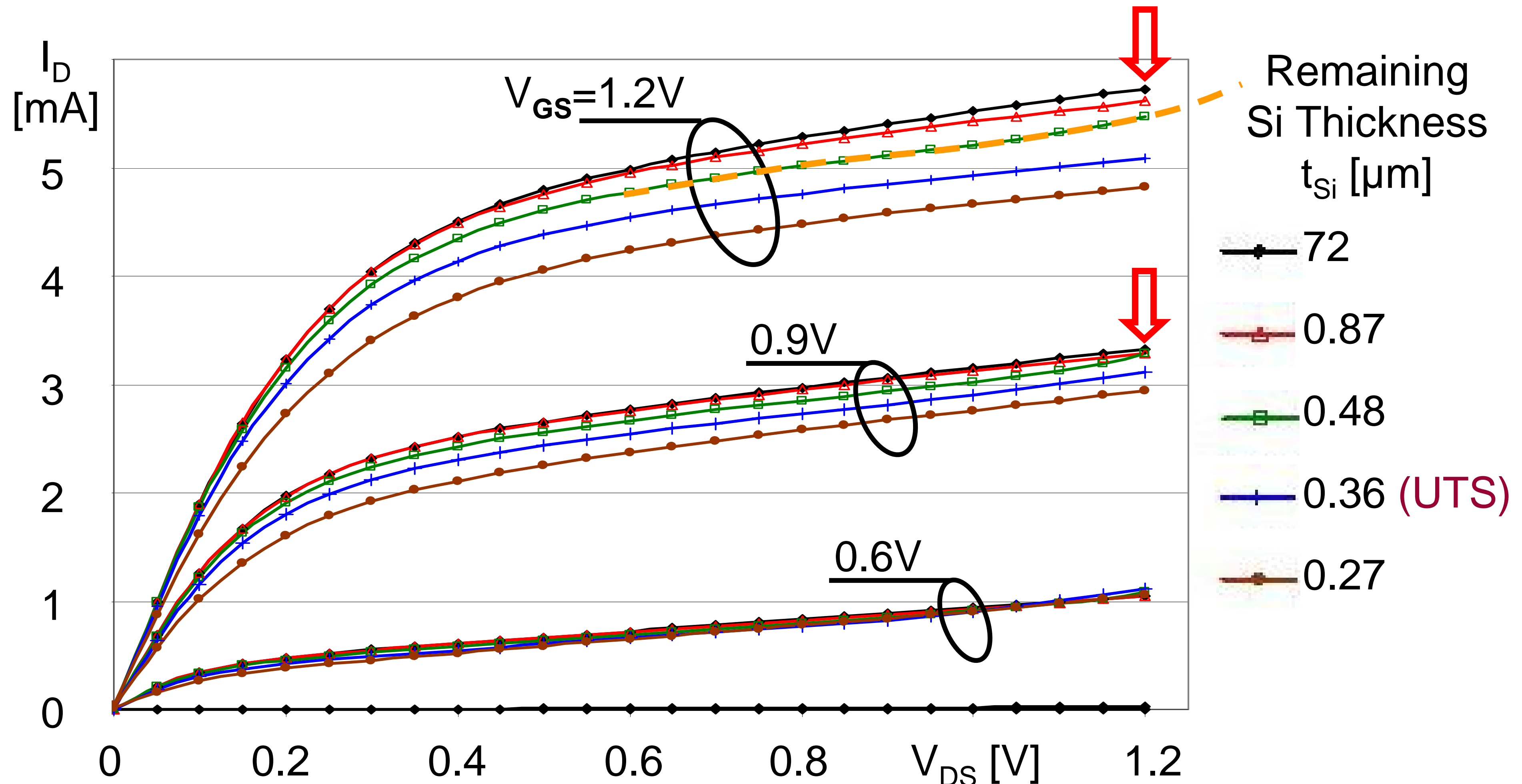
surface near region with:
- crystal defects
- reduced mobility
- increased recombination



Output-Characteristic with FIB Thinning

120nm single n-FET
(measurements all in-situ)

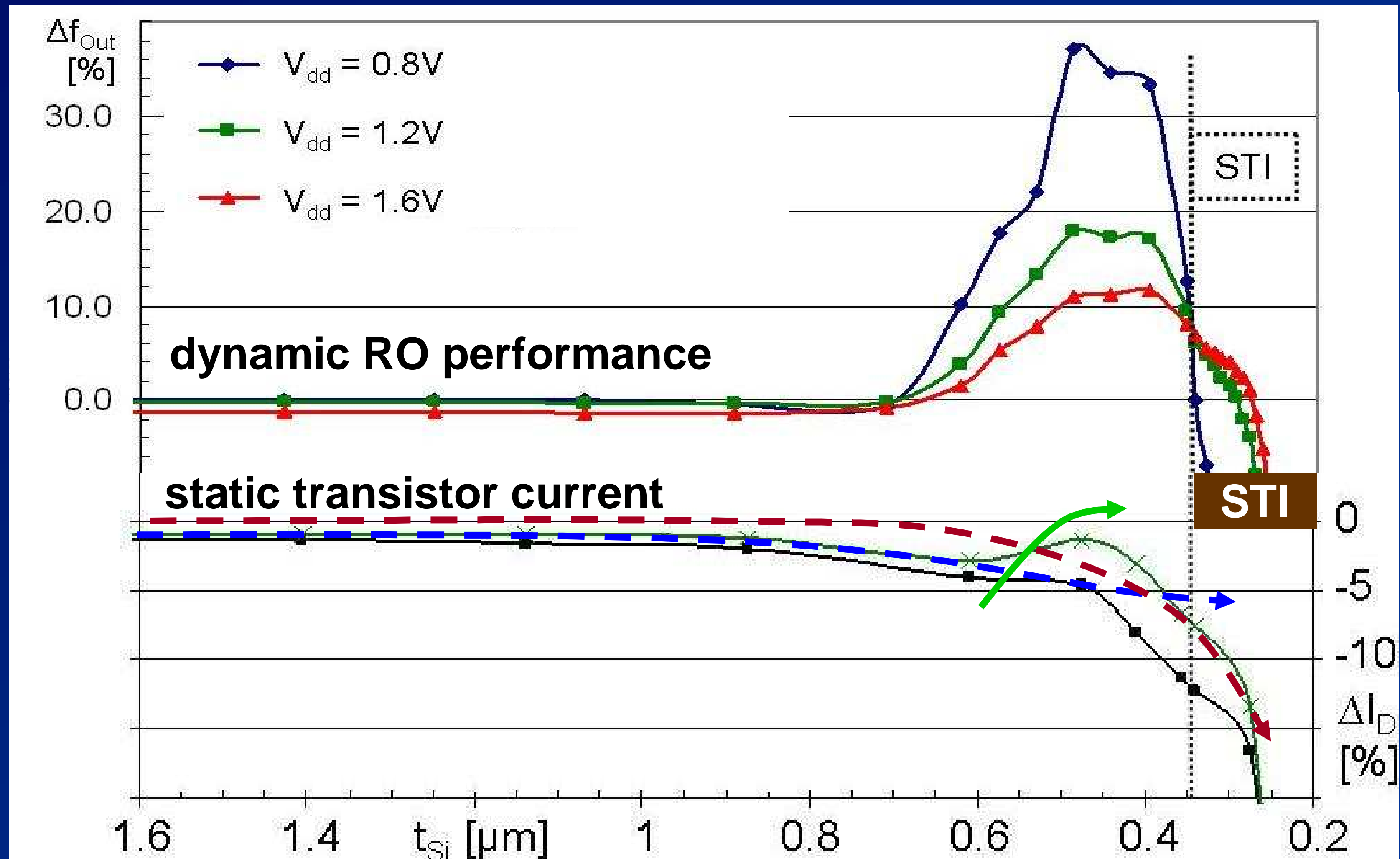
- **~12% $I_{D\,max}$ degradation (UtS)**
- **small kink at t_{Si} ~ 480nm**



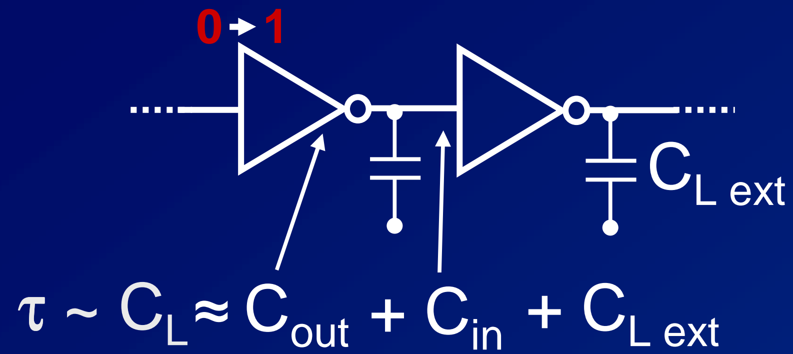
ΔI_D and V_t with FIB Thinning

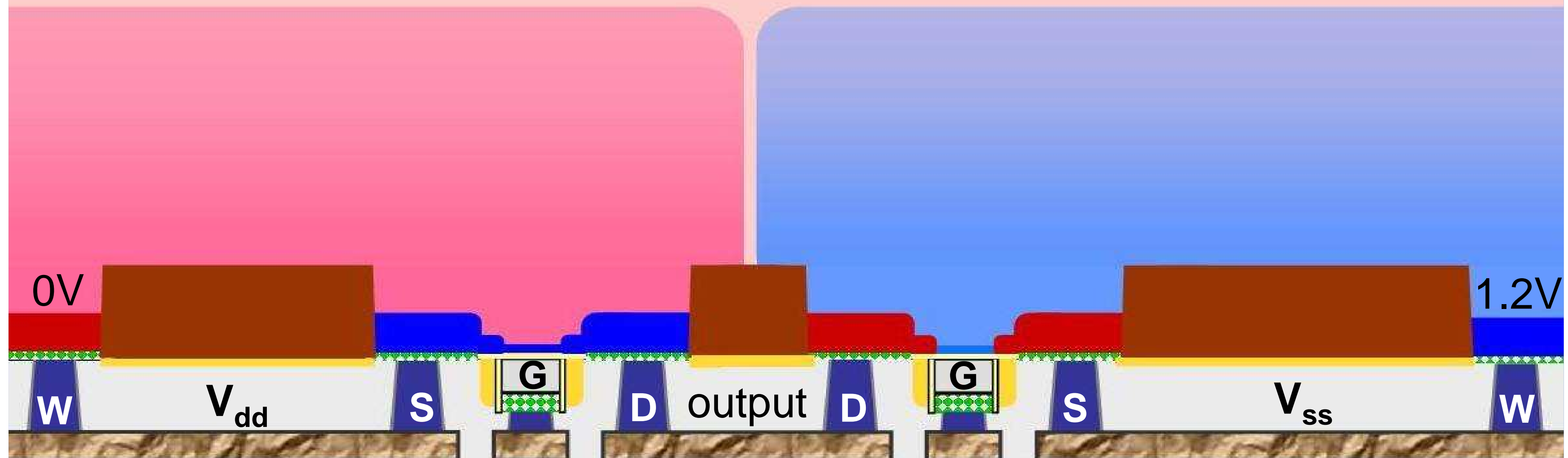
physical device simulations: → increased self-heating (~ 6%)

→ channel mobility (~ 7%) → increasing R_{well} / Kink (≤ +4%)



Dynamic Effects of FIB Thinning





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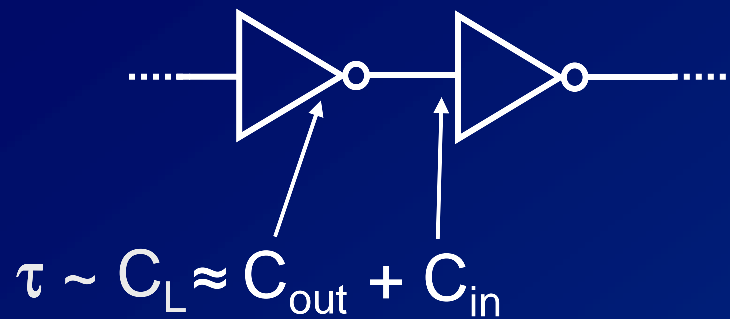
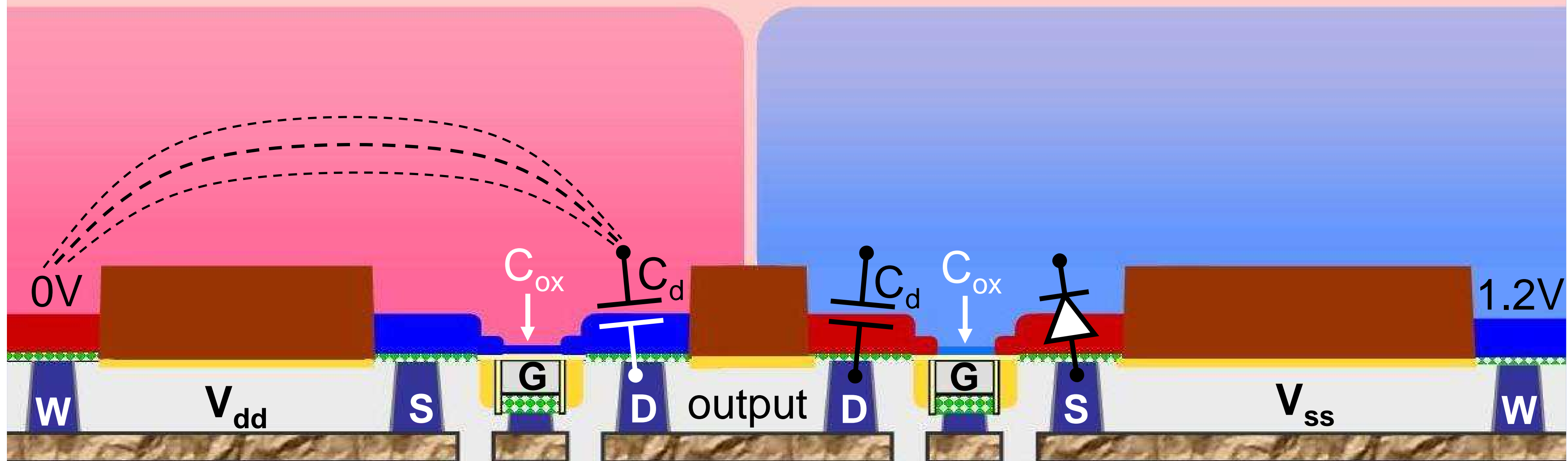


$\tau \sim C_L \approx C_{out} + C_{in}$

$C_{in} \approx \Sigma\, C_{ox}$ (≈ 75%) $C_{out} \approx \Sigma\, C_d$ (≈ 25%)



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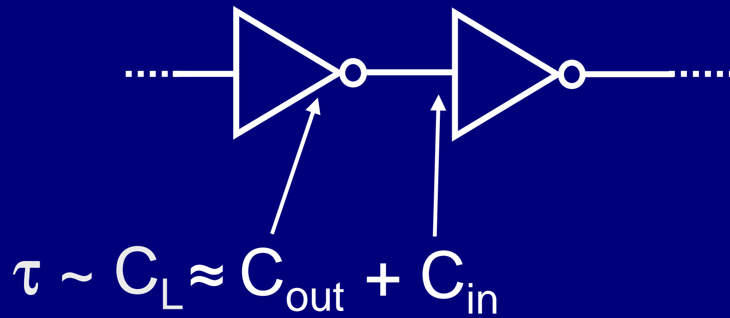

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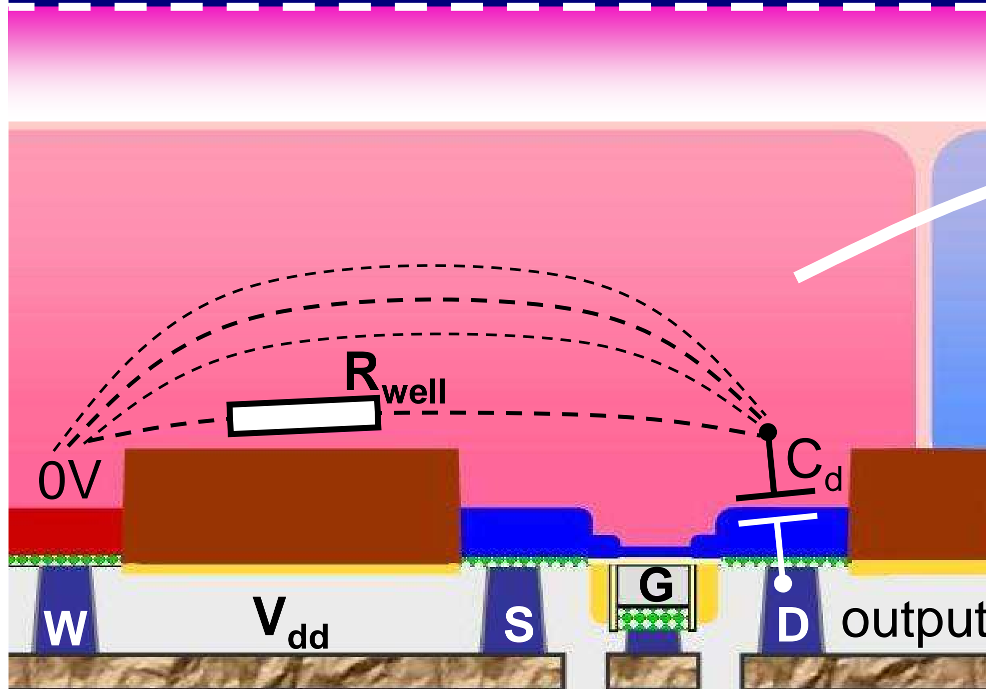
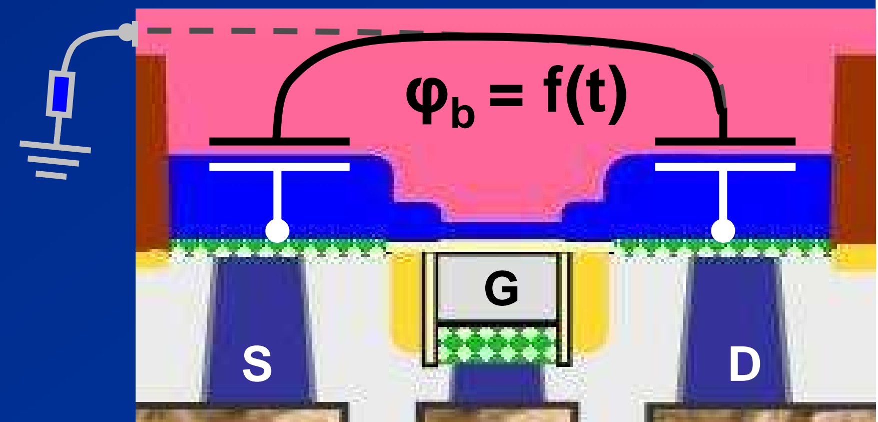


1. **Load reduction ≥ 10%**

$$C'_d \rightarrow \frac{C_d \cdot C_s}{C_d + C_s} \approx 0.55\, C_d$$

$$\rightarrow C'_L < 0.9\, C_L$$



Dynamic Effects of FIB Thinning

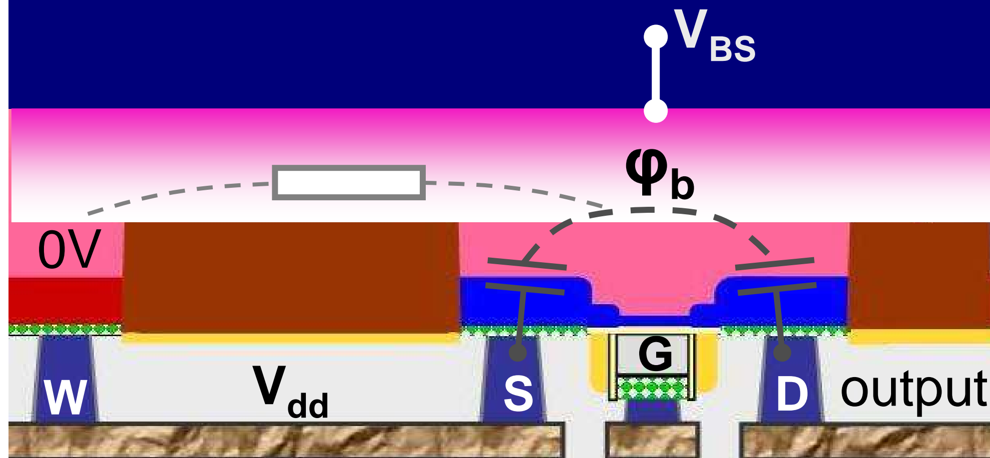
n-FET ⟺ falling edge (off output)

p-FET ⟺ rising edge is equivalent

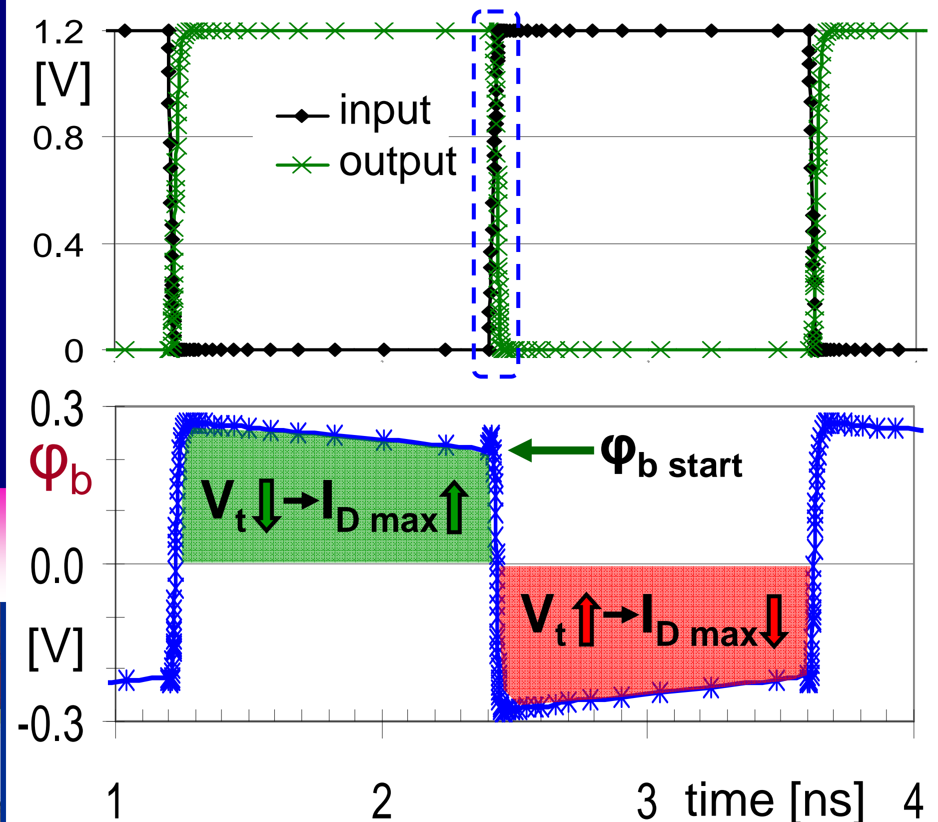
1. Load reduction ≥ 10%
2. "dynamic" V_t reduction

$\varphi_{b\ start} >> 0 \rightarrow V_{t\ start}$ ⇩ & $I_{D\ max}$ ⇧

$$V_t \cong A + \sqrt{B - C \cdot V_{BS}}$$



physical device simulations



Dynamic Effects of FIB Thinning

well diode degradation

→ well to well leakage

1. Load reduction ≥ 10%
2. "dynamic" V_t reduction

initial conditions

0V 1.2V

R_{leak}

0V 1.2V

W V_{dd} S G D output D G S V_{ss} W

Dynamic Effects of FIB Thinning

well diode degradation

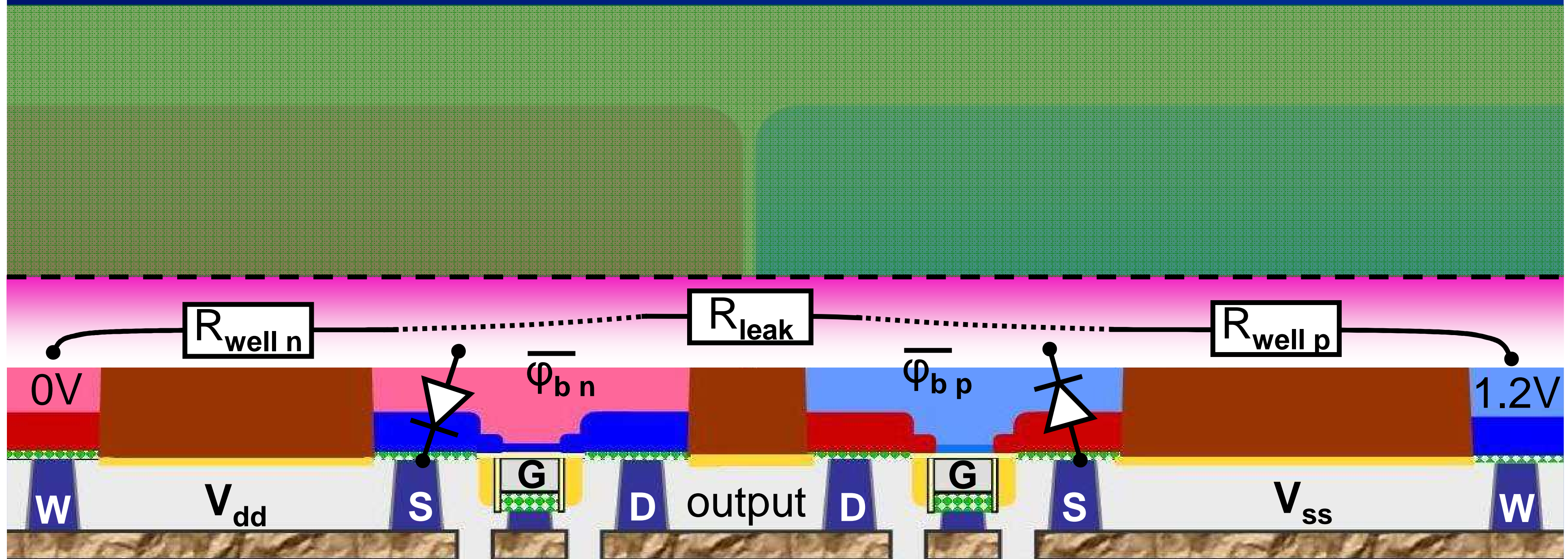
→ well to well leakage

$0 \ll \overline{\varphi_{b\,n}} \leq 0.3V$

$1.2V \gg \overline{\varphi_{b\,p}} \geq 0.9V$

} V_t ↓

1. Load reduction ≥ 10%
2. "dynamic" V_t reduction
3. "static" V_t reduction



Dynamic Effects of FIB Thinning

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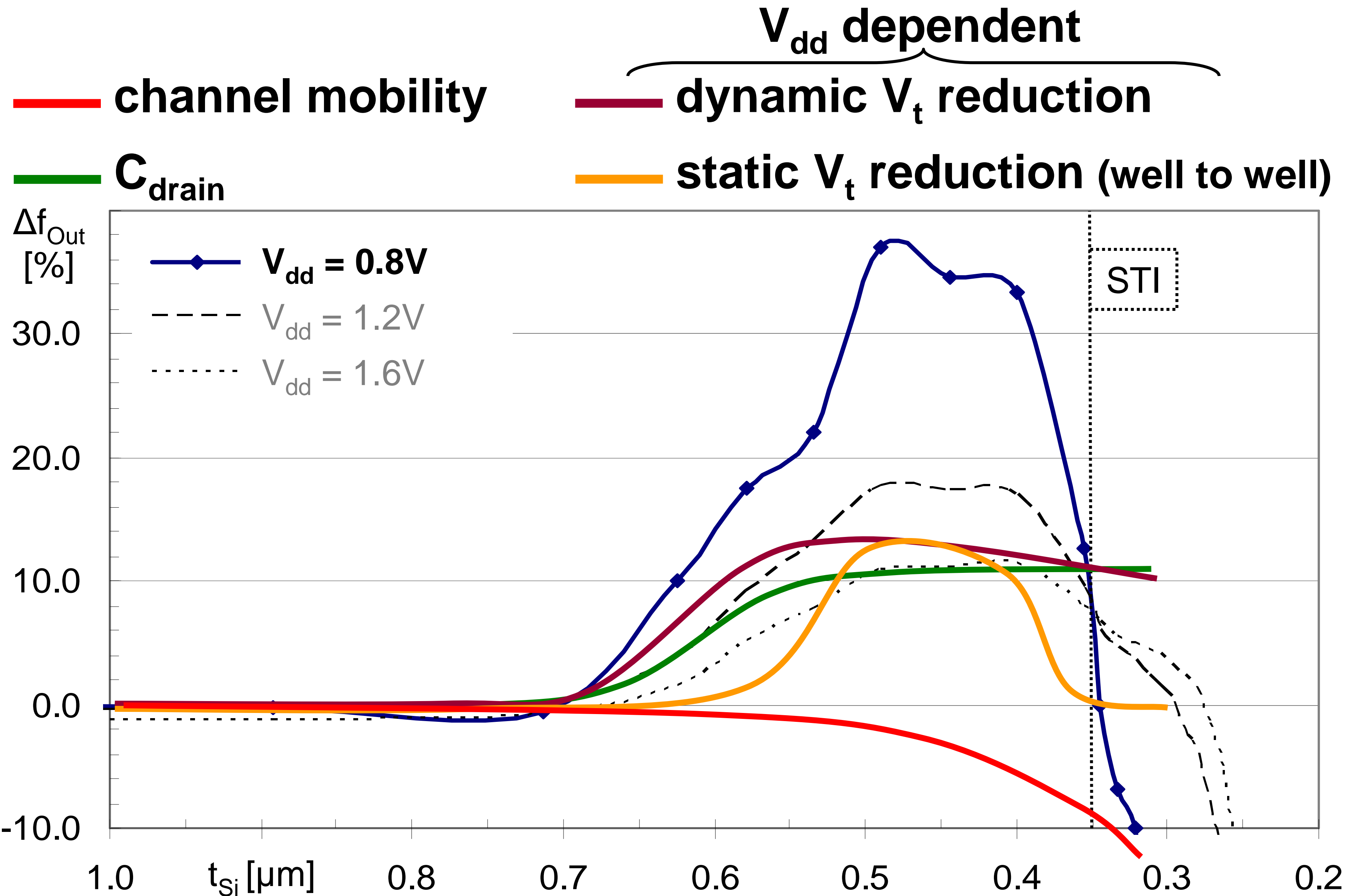
} V_t ↓

1. Load reduction ≥ 10%
2. "dynamic" V_t reduction
3. "static" V_t reduction

→ effect ends with removal of junction

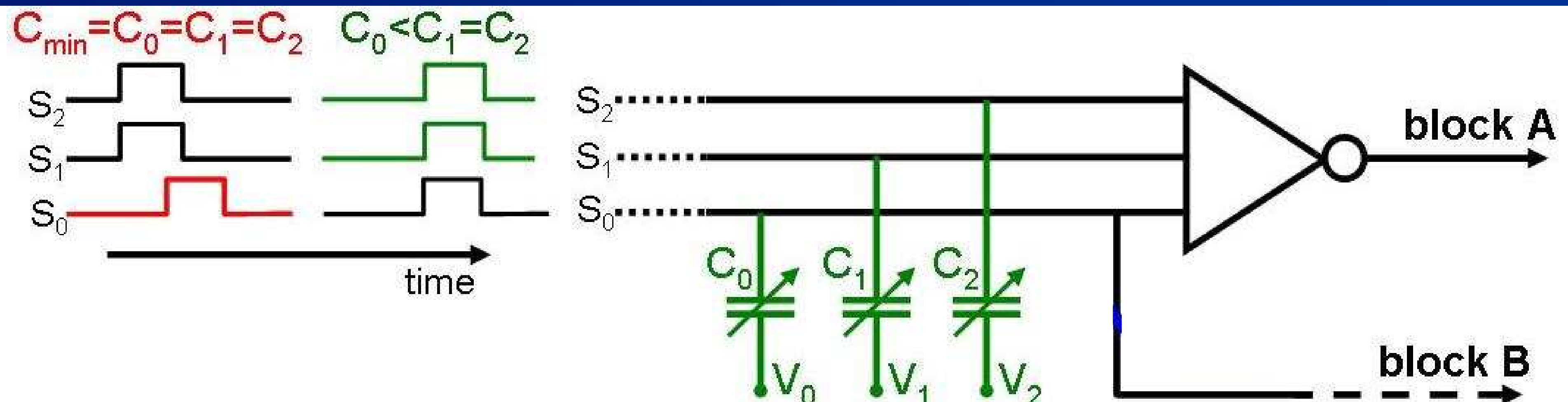
Summary of Dynamic Effects



Application for FA & Debug

- slow branch (+20ps) causes a timing conflict

area overhead => too often not there when needed

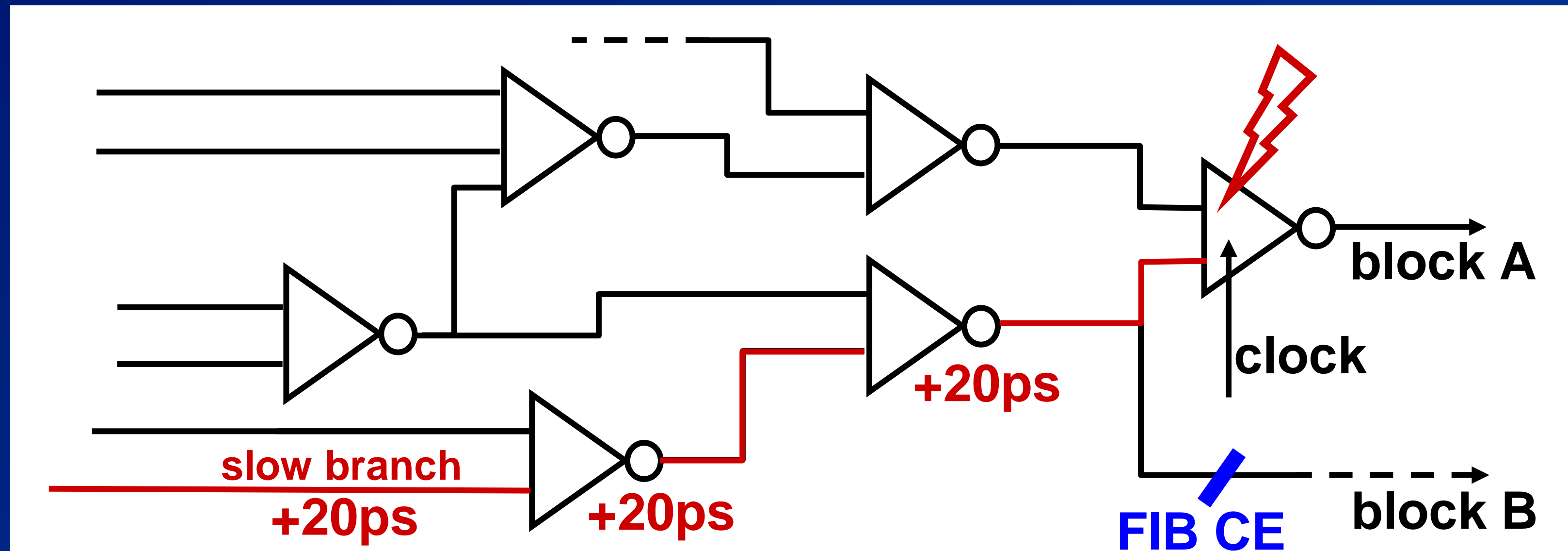


Application for FA & Debug

- slow branch (+20ps) causes a timing conflict
- load reducing FIB CE ⇨ Chip partly dysfunctional
- 20% speed-up with FIB Prep. (-6ps)

  ⇨ applicable to any gate, cell or circuit block

Allows for High Speed Testing of Engineering Samples



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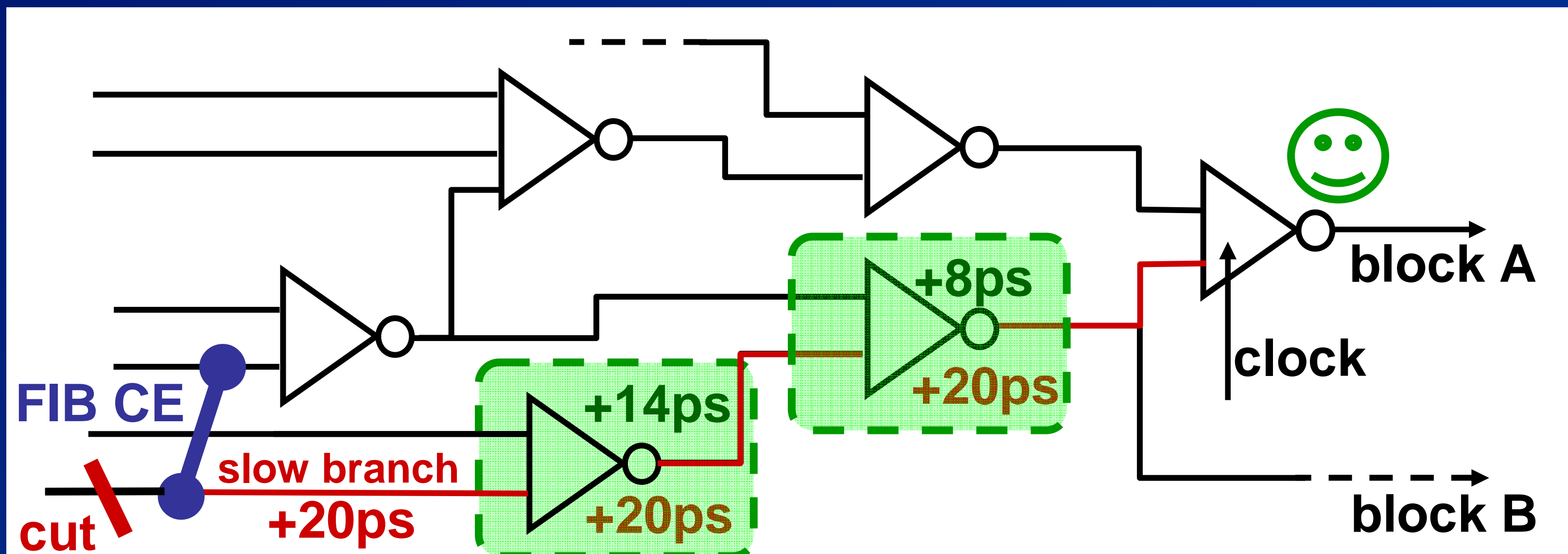
Allows for High Speed Testing of Engineering Samples

- Can equalize CE distortions
- Limited by Cooling !?



Summary

- Optical planarity and thickness control
  - faster throughput / higher success rate

Backside FIB to UtS allows:

- highest alignment accuracy (small STI openings)
- fine-tuning of critical IC timing with full functionality
  - without pre-designed fuses, varactors or load reducing CE
  - controlled and reproducible process
- Full model of the FIB impact on DC & RF performance

  DC ≈ -10% on UtS, RF +10% ⮚ +40%

Discussion

- targeted mechanical prep. thickness 10-100µm ?
- use of optics whilst trenching to n-well ?
- power-up DUT in FIB ?
- STI exposure for alignment ?
  - required alignment accuracy
- Ultra thin Silicon for timing adjustment
  - thermal problems? applicable? necessary?

Special Thanks to

Infineon PFA, Munich

DCG Systems, Fremont

and Christian Boit !

Any Questions ???